## Description

The 5X2503 MicroClock is a programmable clock generator and is intended for low-power, consumer, wearable and smart devices.

The 5X2503 device is a 3 PLL architecture design. Each PLL is individually programmable, allowing for up to 3 unique frequency outputs. The 5X2503 has built-in unique features such as Proactive Power Saving (PPS) to deliver better system-level power management.

An internal OTP memory allows the user to store the configuration in the device without programming after power up. It can then be reprogrammed again through the I$^2$C interface.

The device has programmable VCO and PLL source selection allowing the user to do power-performance optimization based on the application requirements. A low-power 32.768kHz clock is supported with only less than 2μA current consumption for system RTC reference clock needs.

## Typical Applications

- SmartDevice, Handheld, Wearable applications
- Consumer application crystal replacement

## Features

- Configurable OE1 pin function as OE, PPS or DFC control function
- PPS: Proactive Power Saving features save power during the end device power-down mode
- DFC: Dynamic Frequency Control feature allows programming up to 4 difference frequencies that switch dynamically
- Integrated 26MHz crystal; no external input source requirement
- Spread spectrum clock support to lower system EMI
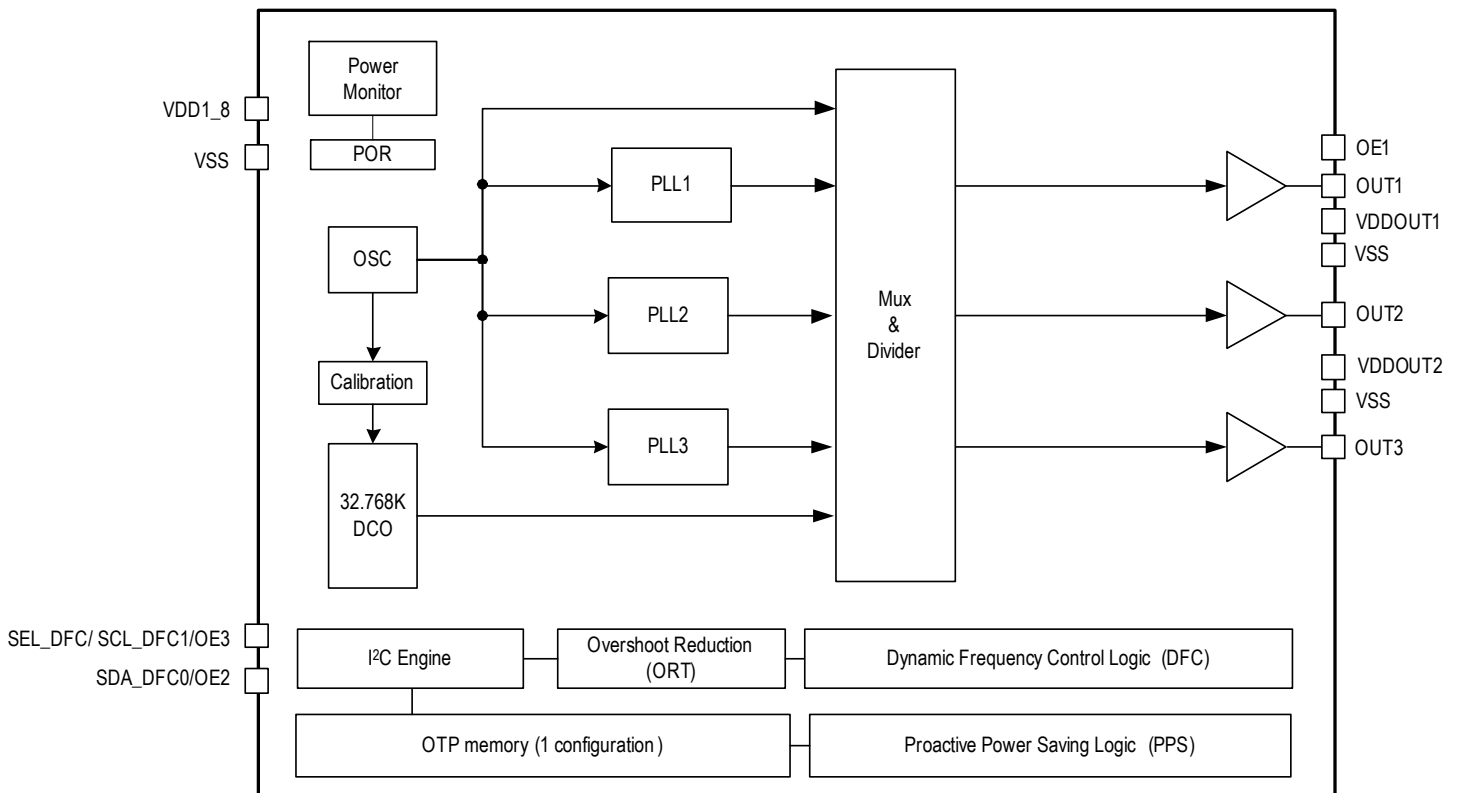- I$^2$C Interface

## Output Features

- 3 LVCMOS outputs, 1MHz–125MHz
- Low-power 32.768kHz clock supported
- Wireless clock crystal integration and fan-out directly

## Key Specifications

- 2μA operation for RTC clock 32.768kHz output
- 2.5 × 2.5 mm 12-DFN with crystal integration; small-form-factor package

## Block Diagram

## Power Group

| Power Supply | SE | DIV | MUX | PLL | DCO | Xtal |
|---|---|---|---|---|---|---|
| $V_{DDOUT1}$ | OUT1 | — | — | — | — | — |
| $V_{DDOUT2}$ | OUT2/OUT3 | — | — | V | — | — |
| $V_{DD1\_8}$ | | V | V | — | V | V |

## Output Source Selection Register Setting Tables

| OUT3 Source | B35b7 | B35b6 |
|---|---|---|
| Divider 3 (DIV3) | 0 | 0 |
| Divider 5 (DIV5) | 0 | 1 |
| Divider 1 (DIV1) | 1 | 0 |
| 32.768kHz DCO | 1 | 1 |

| OUT2 Source | B35b5 | B35b4 |
|---|---|---|
| Divider 3 (DIV3) | 0 | 0 |
| Divider 5 (DIV5) | 0 | 1 |
| Divider 1 (DIV1) | 1 | 0 |
| 32.768kHz DCO | 1 | 1 |

| OUT2 Source | B35b3 | B35b2 |
|---|---|---|
| Divider 3 (DIV3) | 0 | 0 |
| Divider 5 (DIV5) | 0 | 1 |
| Divider 1 (DIV1) | 1 | 0 |
| 32.768kHz DCO | 1 | 1 |

| DIV1 Source | B35b7 | B35b6 |
|---|---|---|
| PLL1 | 0 | 0 |
| DIV4 seed | 1 | X |

# Pin Assignments

**Figure 1. Pin Assignments for 2.5 × 2.5 mm 12-DFN Package**

```
SDA_DFC0/OE2          1     12     V_SS
SEL_DFC/SCL_DFC1/OE3  2     11     OUT3
V_SS                  3     10     V_DDOUT2
V_SS                  4      9     OUT2
V_DD1_8               5      8     OE1
V_DDOUT1              6      7     OUT1
```

2.5 × 2.5 mm 12-DFN
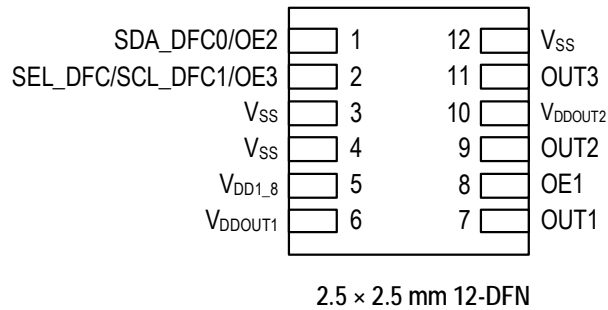
# Pin Descriptions

**Table 1. Pin Descriptions**

| Number | Name | Type | Description |
|--------|------|------|-------------|
| 1 | SDA_DFC0/OE2 | I/O | $I^2C$ data pin; can be DFC0 function by OTP programming or selected by SEL_DFC at power-on default. Output enable pin for OUT2. |
| 2 | SEL_DFC/SCL_DFC1/OE3 | Input | $I^2C$ clock pin; can be DFC1 function by OTP programming selected by SEL_DFC at power-on default. Output enable pin for OUT3. |
| 3 | $V_{SS}$ | Power | Ground pin. |
| 4 | $V_{SS}$ | Power | Ground pin. |
| 5 | $V_{DD1\_8}$ | Power | 1.8V power rail. |
| 6 | $V_{DDOUT1}$ | Power | 1.2V / 1.8V output clock power supply pin; supports OUT1. |
| 7 | OUT1 | Output | 1.2V / 1.8V LVCMOS clock output. |
| 8 | OE1 | Input | Output enable control 1. |
| 9 | OUT2 | Output | 1.8V LVCMOS clock output. |
| 10 | $V_{DDOUT2}$ | Power | 1.8V output clock power supply pin; supports OUT2/3. |
| 11 | OUT3 | Output | 1.8V LVCMOS clock output. |
| 12 | $V_{SS}$ | Power | Ground pin. |
| – | EPAD | GND | Connect to ground pad. |

# Device Feature and Function

## DFC – Dynamic Frequency Control

- OTP programmable–4 different feedback fractional dividers (4 VCO frequencies) that apply to PLL2.
- ORT (overshoot reduction) function will be applied automatically during the VCO frequency change.
- Smooth frequency incremental or decremental from current VCO to targeted VCO base on DFC hardware pins selection.
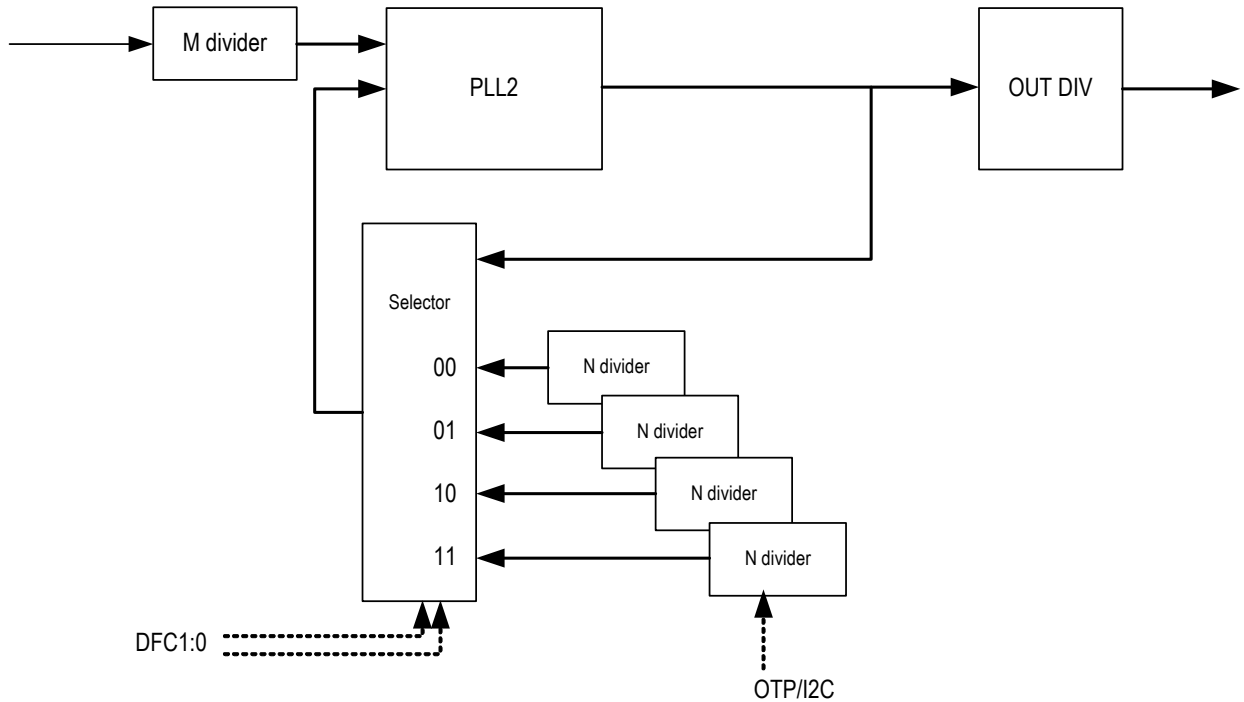
**Figure 2. DFC Function Block Diagram**



**Table 2. DFC Function Priority**

| DFC Mode | OE Pins | DFC_EN bit (W32[4]) | OE1_fun_sel | I$^2$C Pins | SCL_DFC1 | SDA_DFCO | DFC[1:0] | Notes |
|---|---|---|---|---|---|---|---|---|
| Off | OE In* | 0 | 00 or 01 or 10* | Active (SCL = 1 at POR) | SCL Input | SDA I/O | N/A | DFC disable |
| On | DFC0 In | 1 | 11 | Active | SCL Input | SDA I/O | DFC0 = OE | One pin DFC via OE1 |
| On | OE In* | 1 | 00 or 01 or 10* | Inactive (SCL = 0 at POR) | DFC1 | DFC0 | DFC1 = SCL_DFC1 | I$^2$C pin as DFC control pins |
| On | OE In* | 1 | 00 or 01 or 10* | Active (SCL = 1 at POR) | SCL Input | SDA I/O | W30[1:0] | I$^2$C control DFC mode |

\* See *OE Pin Function* table.

## DFC Function Programming

- Register B63b3:2 selects DFC00–DFC11 configuration.
- Byte16–19 are the registers for PLL2 VCO setting, based on B63b3:2 configuration selection, the data write to B16–19 will be stored in selected configuration OTP memory.
- Refer to *DFC Function Priority* table. Select proper control pin(s) to activate DFC function.
- Note the DFC function can also be controlled by I$^2$C access.

## PPS – Proactive Power Saving Function

PPS (Proactive Power Saving) is an IDT patented unique design for the clock generator that proactively detects end device power down state and then switches output clocks between normal operation clock frequency and low power mode 32kHz clock that only consumes < 5µA current. The system could save power when the device goes into power down or sleep mode. The PPS function diagram is shown as below.

**Figure 3. PPS Function Block Diagram**
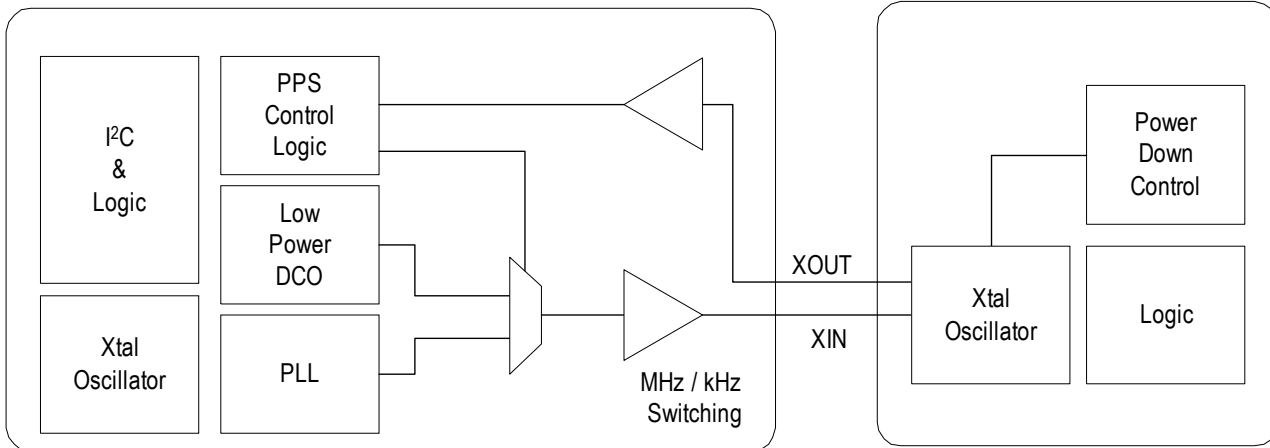


**Figure 4. PPS Assertion/Deassertion Timing Chart**
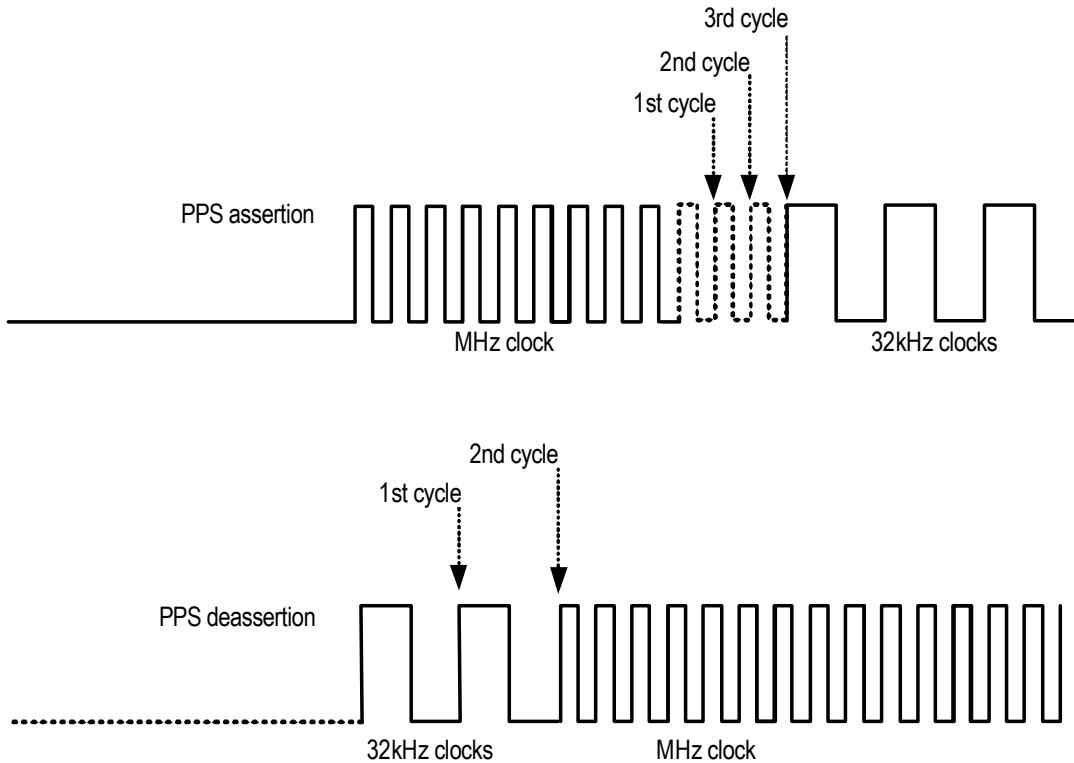


## PPS Function Programming

Refer to the *OE Pin Function* table to have proper PPS function selected for OE pin(s). Note that the register default is set to Output Enable (OE) function for OE pins.

## Input Pin Function

The input pins in 5X2503 have multiple functions. The OE1 pin can be configured as output enable control (OE) or chip power-down control (PD#) or Proactive Power Saving function (PPS). Furthermore, the OE1 pin can be configured as single or Dynamic Frequency Control (DFC).

SCL/SDA are also multiple function pins. The two pins can be configured as output enable control (OE), or I$^2$C interface or Dynamic Frequency Control (DFC) functions by programming and hardware pin latch.

**Table 3.  OE1 Pin Function Table**

| Function | Byte30 | |
|---|---|---|
| | bit6 | bit5 |
| OUT1 Output Enable/Disable | 0 | 0 |
| Global Power Down (PD#) | 0 | 1 |
| OUT1 Proactive Power Saving Input (OUT1 PPS) | 1 | 0 |
| DFC0 | 1 | 1 |

**Table 4.  SDA/SCL Function Selection**

| SEL_DFC (latched) | Enable OE2/3 B36<2> | DFC_EN B32<4> | OE1 Funsel B30<6:5> | Function of SCL/SDA |
|---|---|---|---|---|
| 0 | 0 | 0 | 00, 01, 10 | NA |
| 0 | 0 | 1 | 00, 01, 10 | SCL = DFC1, SDA = DFC0 |
| 0 | 1 | X | 00, 01, 10 | SCL = OE3, SDA = OE2 |
| 1 | X | X | 00, 01, 10 | SCL, SDA |

# Spread Spectrum

The 5X2503 supports spread spectrum clocks from PLL1. PLL1 has built-in analog spread spectrum; PLL2 and PLL3 use seed clock from PLL1.

# ORT – VCO Overshoot Reduction Technology

The 5X2503 supports innovate the VCO overshoot reduction technology to prevent the output clock frequency spike when the device is change frequency on the fly or doing DFC (Dynamic Frequency Control) function.

The VCO frequency change are under control instead of free run to targeted frequency.

# PLL Features and Descriptions

**Table 5.  Output Divider 1**

| Output Divider Bits [1:0] | Output Divider Bits [3:2] | | | |
|---|---|---|---|---|
| | 00 | 01 | 10 | 11 |
| 00 | 1 | 2 | 4 | 8 |
| 01 | 4 | 8 | 16 | 32 |
| 10 | 5 | 10 | 20 | 40 |
| 11 | 6 | 12 | 24 | 48 |

**Table 6.  Output Divider 2, 3, and 5**

| Output Divider Bits [1:0] | Output Divider Bits [3:2] | | | |
|:---:|:---:|:---:|:---:|:---:|
| | 00 | 01 | 10 | 11 |
| 00 | 1 | 2 | 4 | 5 |
| 01 | 3 | 6 | 12 | 15 |
| 10 | 5 | 10 | 20 | 25 |
| 11 | 10 | 20 | 40 | 50 |

**Table 7.  Output Divider 4**

| Output Divider Bits [1:0] | Output Divider Bits [3:2] | | | |
|:---:|:---:|:---:|:---:|:---:|
| | 00 | 01 | 10 | 11 |
| 00 | 1 | 2 | 4 | 8 |
| 01 | 3 | 6 | 12 | 24 |
| 10 | 5 | 10 | 20 | 40 |
| 11 | 10 | 20 | 40 | 80 |

# Output Clock Test Conditions

**Figure 5.  LVCMOS Output Clock Test Condition**
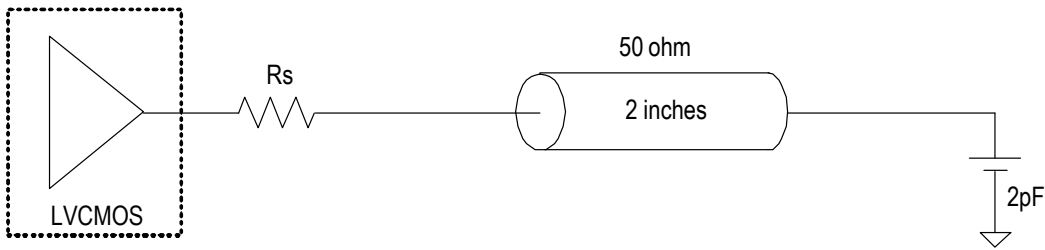


| $V_{DDO}$ | $R_{OUT}$ | Rs |
|:---:|:---:|:---:|
| 1.2V | 30Ω | 20Ω |
| 1.8V | 17Ω | 33Ω |

# Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5X2503. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

**Table 8. Absolute Maximum Ratings**

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD1\_8}$, $V_{DDOUTx}$ | 1.89V |
| Inputs | |
| Other Inputs | -0.5V to $V_{DD1\_8}$ / $V_{DDOUTx}$ |
| Outputs, $V_{DDOUTx}$ (LVCMOS) | -0.5V to $V_{DDOUTx}$ + 0.5V |
| Outputs, IO (SDA) | 10mA |
| Package Thermal Impedance, $\Theta_{JA}$ | 42°C/W (0mps) |
| Package Thermal Impedance, $\Theta_{JC}$ | 41.8°C/W (0mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |
| ESD Human Body Model | 2000V |
| Junction Temperature | 125°C |

# Recommended Operating Conditions

**Table 9. Recommended Operating Conditions**

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $V_{DDOUT1}$ | Power Supply Voltage for Supporting OUT1 | 1.71 | 1.8 | 1.89 | V |
| $V_{DDOUT1}$ | Power Supply Voltage for Supporting OUT1 | 1.14 | 1.2 | 1.26 | V |
| $V_{DDOUT2}$ | Power Supply Voltage for Supporting OUT2/OUT3 | 1.71 | 1.8 | 1.89 | V |
| $V_{DD1\_8}$ | Power Supply Voltage for Core Logic Functions | 1.71 | 1.8 | 1.89 | V |
| $T_A$ | Ambient Operating Temperature | -40 | — | 85 | °C |
| $C_{LOAD\_OUT}$ | Maximum Load Capacitance (1.8V LVCMOS only) | — | 5 | — | pF |
| $t_{PU}$ | Power-up Time for all $V_{DD}$s to reach Minimum Specified Voltage (power ramps must be monotonic) | 0.05 | — | 3 | ms |

## Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance ($T_A$ = +25 °C)

**Table 10. Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance**

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance (OE, SDA, SCL) | — | 3 | 7 | pF |
| Pull-down Resistor | OE | — | 150 | — | kΩ |
| $R_{OUT}$ | LVCMOS Output Driver Impedance ($V_{DDOUTx}$ = 1.8V) | — | 17 | — | Ω |

# Integrated Crystal Characteristics

**Table 11. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | — | | Fundamental | | |
| Frequency | — | — | 26 | — | MHz |
| Frequency Tolerance (25°C)[1] | — | -20 | — | 20 | ppm |
| Equivalent Series Resistance (ESR) | — | — | 10 | 100 | Ω |
| Shunt Capacitance | — | — | 2 | 7 | pF |
| Load Capacitance ($C_L$) | — | 6 | 8 | 10 | pF |
| Maximum Crystal Drive Level | — | — | — | 100 | µW |

[1] Frequency deviation–refer to center frequency.

# DC Electrical Characteristics

**Table 12. DC Electrical Characteristics [1,2]**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Operation Supply Current | $V_{DD}$ = $V_{DDOUTx}$ = $V_{DD1\_8}$ = 1.8V; OUT1 = 12MHz, OUT3 = 26MHz, OUT2 off, no load. | — | 2.0 | — | mA |
| | | $V_{DD}$ = $V_{DDOUTx}$ = $V_{DD1\_8}$ = 1.8V; OUT1 = 12MHz, OUT3 = 26MHz, OUT2 off, with load. | — | 3.5 | — | mA |
| | | $V_{DD}$ = $V_{DDOUTx}$ = $V_{DD1\_8}$ = 1.8V; OUT1 = 26MHz, OUT3 = 26MHz, OUT2 = 32kHz, no load. | — | 1.8 | — | mA |
| | | $V_{DD}$ = $V_{DDOUTx}$ = $V_{DD1\_8}$ = 1.8V; OUT1 = 26MHz, OUT3 = 26MHz, OUT2 = 32kHz, with load. | — | 3.8 | — | mA |
| $I_{DDPD}$ | Power Down Current | PD asserted with $V_{DD1\_8}$ and $V_{DDOUTx}$ on, I²C programming, 32kHz running. | — | 390 | — | µA |
| $I_{DDSUSPEND}$ | Power Suspend Current | $V_{DDOUT2}$ off and only $V_{DDOUT1}$ and $V_{DD1\_8}$ on, I²C programming, 32kHz running. | — | 1.6 | 2.0 | µA |

[1] Single CMOS driver active.

[2] OUT1–3 current measured with 0.5 inches transmission line and no load.

# Electrical Characteristics–Input Parameters

Supply Voltage $V_{DD1\_8}$ = 1.8V ±5%, $V_{DDOUTx}$ = 1.8V ±5%, $T_A$ = -40°C to +85°C.

**Table 13. Electrical Characteristics–Input Parameters [1]**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|------------|---------|---------|---------|-------|
| $I_{IL}$ | Input Leakage Low Current for OE1 | $V_{IN}$ = GND at OE1 pin. | 150 | — | 5 | µA |
| $I_{IH}$ | Input Leakage High Current for OE1 | $V_{IN}$ = 1.89V. | — | — | 20 | µA |
| $I_{\_OE1}$ | Input Leakage Current | $V_{IN}$ = 1.89V at OE1 pin. | — | — | 120 | µA |

[1] Guaranteed by design and characterization; test in production.

# DC Electrical Characteristics for 1.8V LVCMOS

$V_{DD}$ = 1.8V ±5%, $V_{DDOUTx}$ = 1.8V ±5%, $T_A$ = -40°C to 85°C.

**Table 14. DC Electrical Characteristics – 1.8V LVCMOS**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|------------|---------|---------|---------|-------|
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -8mA. | $0.7 \times V_{DDOUTx}$ | — | $V_{DDOUTx}$ | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8mA. | — | — | $0.25 \times V_{DDOUTx}$ | V |
| $I_{OZDD}$ | Output Leakage Current | Tri-state outputs, $V_{DDOUTx}$ = 1.89V. | — | — | 3 | µA |
| $V_{IH}$ | Input High Voltage | Single-ended inputs – OE, SDA, SCL. | $0.65 \times V_{DDOUTx}$ | — | $V_{DDOUT}x + 0.3$ | V |
| $V_{IL}$ | Input Low Voltage | Single-ended inputs – OE, SDA, SCL. | GND - 0.3 | — | $0.35 \times V_{DDOUTx}$ | V |

# AC Electrical Characteristics

**Table 15. AC Timing Electrical Characteristics – 32.768kHz**

$V_{DD1\_8}$ = 1.8V ±5%, $V_{DDOUTx}$ = 1.8V ±5%, $T_A$ = -40°C to +85°C; spread spectrum = off.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|------------|---------|---------|---------|-------|
| $f_{OUT}$ | Initial Frequency | Single-ended clock output limit (LVCMOS). | | 32.768 | | kHz |
| $f_{OUT\_tor}$[1] | Frequency Tolerance | At 25°C. | -20 | | 20 | ppm |
| t1 | Output Duty Cycle | Measured at 50%. | 45 | | 55 | % |

[1] This measurement uses a 3-day average.

**Table 16. AC Timing Electrical Characteristics – 1.8V**

$V_{DD1\_8}$ = 1.8V ±5%, $V_{DDOUTx}$ = 1.8V ±5%, $T_A$ = -40°C to +85°C; spread spectrum = off.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | Single-ended clock output limit (LVCMOS). | 1 | — | 125 | MHz |
| t1 | Output Duty Cycle | LVCMOS clock < 120MHz. | 45 | — | 55 | % |
| t2 | Rise/Fall Time | Single-ended LVCMOS output clock rise and fall time, 20% to 80% of $V_{DDOUT}$ 1.8V. | — | 1.0 | 1.5 | ns |
| t3 | Clock Jitter | Cycle-to-cycle jitter (peak-to-peak), multiple output frequencies switching, differential outputs (1.8V nominal output voltage). OUT1 = 25MHz. OUT2 = 100MHz. OUT3 = 125MHz. | — | 50 | 200 | ps |
| | | Cycle-to-cycle jitter (peak-to-peak), multiple output frequencies switching, differential outputs (1.8V nominal output voltage). OUT1 = 24MHz. OUT2 = 32.768kHz. OUT3 = 26MHz. | — | 50 | 200 | ps |
| | | Cycle-to-cycle jitter (peak-to-peak), multiple output frequencies switching, differential outputs (1.8V nominal output voltage). OUT1 = 32.768kHz. OUT2 = 26MHz. OUT3 = 26MHz. | — | 50 | 200 | ps |
| t5 [2] | Lock Time | PLL lock time from power-up. | — | | 20 | ms |
| t6 | Lock Time | 32.768kHz clock low-power, power-up time. | — | 10 | 100 | ms |
| t6 [3] | Lock Time | PLL lock time from shutdown mode. | — | 0.1 | 2 | ms |

[1] Practical lower frequency is determined by loop filter settings.

[2] Includes loading the configuration bits from OTP to PLL registers. It does not include OTP programming/write time.

[3] Actual PLL lock time depends on the loop configuration.

**Table 17. AC Timing Electrical Characteristics, 1.2V / 1.8V**

$V_{DD1\_8}$ = 1.8V ±5%, $V_{DDOUT1}$ = 1.2V ±5%, $V_{DDOUT2}$ = 1.8V ±5%, $T_A$ = -40°C to +85°C; spread spectrum = off.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | Single-ended clock output limit (LVCMOS). | 1 | — | 125 | MHz |
| t1 | Output Duty Cycle | LVCMOS clock < 120MHz. | 45 | — | 55 | % |
| t2 | Rise/Fall Time | OUT2/OUT3 LVCMOS output clock rise and fall time, 20% to 80% of $V_{DDOUT2}$ = 1.8V. | — | 1.0 | 1.5 | ns |
| | | OUT1 LVCMOS output clock rise and fall time, 20% to 80% of $V_{DDOUT1}$ = 1.2V. | — | 1.5 | 2.5 | ns |
| t3 | Clock Jitter | Cycle-to-cycle jitter (peak-to-peak), multiple output frequencies switching, differential outputs (1.8V nominal output voltage; 1.2V on $V_{DDOUT1}$).<br>OUT1 = 25MHz.<br>OUT2 = 100MHz.<br>OUT3 = 125MHz. | — | 100 | 350 | ps |
| | | Cycle-to-cycle jitter (peak-to-peak), multiple output frequencies switching, differential outputs (1.8V nominal output voltage; 1.2V on $V_{DDOUT1}$).<br>OUT1 = 32.768kHz.<br>OUT2 = 26MHz.<br>OUT3 = 26MHz. | — | 50 | 100 | ps |
| t5 [2] | Lock Time | PLL lock time from power-up. | — | | 20 | ms |
| t6 | Lock Time | 32.768kHz clock low-power, power-up time. | — | 10 | 100 | ms |
| t6 [3] | Lock Time | PLL lock time from shutdown mode. | — | 0.1 | 2 | ms |

[1] Practical lower frequency is determined by loop filter settings.

[2] Includes loading the configuration bits from OTP to PLL registers. It does not include OTP programming/write time.

[3] Actual PLL lock time depends on the loop configuration.

# I²C Bus DC Characteristics

**Table 18. I²C Bus DC Characteristics**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Level | — | $0.7 \times V_{DD1\_8}$ | — | — | V |
| $V_{IL}$ | Input Low Level | — | — | — | $0.3 \times V_{DD1\_8}$ | V |
| $V_{HYS}$ | Hysteresis of Inputs | — | $0.05 \times V_{DD1\_8}$ | — | — | V |
| $I_{IN}$ | Input Leakage Current | — | — | — | ±1 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 3 mA. | — | — | 0.4 | V |

**Table 19. I²C Bus AC Characteristics**

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $F_{SCLK}$ | Serial Clock Frequency (SCL) | — | 100 | 400 | kHz |
| $t_{BUF}$ | Bus Free Time between STOP and START | 1.3 | — | — | µs |
| $t_{SU:START}$ | Setup Time, START | 0.6 | — | — | µs |
| $t_{HD:START}$ | Hold Time, START | 0.6 | — | — | µs |
| $t_{SU:DATA}$ | Setup Time, data input (SDA) | 100 | — | — | ns |
| $t_{HD:DATA}$ | Hold Time, data input (SDA) [1] | 0 | — | — | µs |
| $t_{OVD}$ | Output Data Valid from Clock | — | — | 0.9 | µs |
| $C_B$ | Capacitive Load for Each Bus Line | — | — | 400 | pF |
| $t_R$ | Rise Time, data and clock (SDA, SCL) | $20 + 0.1 \times C_B$ | — | 300 | ns |
| $t_F$ | Fall Time, data and clock (SDA, SCL) | $20 + 0.1 \times C_B$ | — | 300 | ns |
| $t_{HIGH}$ | High Time, clock (SCL) | 0.6 | — | — | µs |
| $t_{LOW}$ | Low Time, clock (SCL) | 1.3 | — | — | µs |
| $t_{SU:STOP}$ | Setup Time, STOP | 0.6 | — | — | µs |

[1] A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

# Spread Spectrum Generation Specifications

**Table 20. Spread Spectrum Generation Specifications**

| Symbol | Parameter | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | Output frequency range. | 1 | — | 125 | MHz |
| $f_{MOD}$ | Mod Frequency | Modulation frequency. | 30 to 63 | | | kHz |
| $f_{SPREAD}$ | Spread Value | Amount of spread value (programmable)–down spread. | -0.5% to -2% | | | % $f_{OUT}$ |
| %tolerance | Spread% Value | Variation of spread range. | — | 15 | — | % |

# General SMBus Serial Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) sends the byte count = X
- IDT clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will acknowledge each byte one at a time
- Controller (host) sends a stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | | |
| | | | ACK |
| O | | X Byte | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will acknowledge
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|---|---|---|---|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count=X |
| ACK | | | |
| | | | Beginning Byte N |
| ACK | | X Byte | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

December 18, 2017

**SMBus Table Byte 0: General Control**

| Byte 00h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OTP_Burned | OTP memory programming indication | R/W | OTP memory non-programmed | OTP memory programmed | 0 |
| Bit 6 | I2C_addr[1] | I$^2$C address select bit 1 | R/W | 00: D0 / 01: D2 10: D4 / 11: D6 | | 0 |
| Bit 5 | I2C_addr[0] | I$^2$C address select bit 0 | R/W | — | — | 0 |
| Bit 4 | PLL1_SSEN | PLL1 Spread Spectrum enable | R/W | disable | enable | 0 |
| Bit 3 | Reserved | Reserved | R/W | — | — | 0 |
| Bit 2 | PLL3_refin_sel | PLL3 source selection | R/W | Xtal | Seed (DIV2) | 0 |
| Bit 1 | Reserved | Reserved | R/W | — | — | 0 |
| Bit 0 | OTP_protect | OTP memory protection | R/W | read/write | write locked | 0 |

**SMBus Table Byte 1: Dash Code (optional)**

| Byte 01h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | DashCode ID[7] | Dash code ID | R/W | — | — | 0 |
| Bit 6 | DashCode ID[6] | Dash code ID | R/W | — | — | 0 |
| Bit 5 | DashCode ID[5] | Dash code ID | R/W | — | — | 0 |
| Bit 4 | DashCode ID[4] | Dash code ID | R/W | — | — | 0 |
| Bit 3 | DashCode ID[3] | Dash code ID | R/W | — | — | 0 |
| Bit 2 | DashCode ID[2] | Dash code ID | R/W | — | — | 0 |
| Bit 1 | DashCode ID[1] | Dash code ID | R/W | — | — | 0 |
| Bit 0 | DashCode ID[0] | Dash code ID | R/W | — | — | 0 |

**SMBus Table Byte 2: Crystal Cap Setting**

| Byte 02h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | | Reserved | R/W | — | — | 0 |
| Bit 6 | | Reserved | R/W | — | — | 0 |
| Bit 5 | | Reserved | R/W | — | — | 0 |
| Bit 4 | | Reserved | R/W | — | — | 1 |
| Bit 3 | | Reserved | R/W | — | — | 0 |
| Bit 2 | | Reserved | R/W | — | — | 0 |
| Bit 1 | | Reserved | R/W | — | — | 0 |
| Bit 0 | | Reserved | R/W | — | — | 1 |

## SMBus Table Byte 3: PLL3 M Divider

| Byte 03h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|------|------------------|------|---|---|-----|
| Bit 7 | PLL3_MDIV1 | PLL3 source clock divider | R/W | disable M DIV1 | bypadd divider (/1) | 0 |
| Bit 6 | PLL3_MDIV2 | PLL3 source clock divider | R/W | disable M DIV2 | bypadd divider (/2) | 0 |
| Bit 5 | PLL3 M_DIV[5] | PLL3 reference integer divider | R/W | | | 0 |
| Bit 4 | PLL3 M_DIV[4] | PLL3 reference integer divider | R/W | | | 1 |
| Bit 3 | PLL3 M_DIV[3] | PLL3 reference integer divider | R/W | 3–64, default is 26 | | 1 |
| Bit 2 | PLL3 M_DIV[2] | PLL3 reference integer divider | R/W | | | 0 |
| Bit 1 | PLL3 M_DIV[1] | PLL3 reference integer divider | R/W | | | 1 |
| Bit 0 | PLL3 M_DIV[0] | PLL3 reference integer divider | R/W | | | 0 |

## SMBus Table Byte 4: PLL3 N Divider

| Byte 04h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|------|------------------|------|---|---|-----|
| Bit 7 | PLL3 N_DIV[7] | PLL3 VCO feedback integer divider bit7 | R/W | | | 1 |
| Bit 6 | PLL3 N_DIV[6] | PLL3 VCO feedback integer divider bit6 | R/W | | | 1 |
| Bit 5 | PLL3 N_DIV[5] | PLL3 VCO feedback integer divider bit5 | R/W | | | 1 |
| Bit 4 | PLL3 N_DIV[4] | PLL3 VCO feedback integer divider bit4 | R/W | 12–2048, default VCO setting is 480MHz | | 0 |
| Bit 3 | PLL3 N_DIV[3] | PLL3 VCO feedback integer divider bit3 | R/W | | | 0 |
| Bit 2 | PLL3 N_DIV[2] | PLL3 VCO feedback integer divider bit2 | R/W | | | 0 |
| Bit 1 | PLL3 N_DIV[1] | PLL3 VCO feedback integer divider bit1 | R/W | | | 0 |
| Bit 0 | PLL3 N_DIV[0] | PLL3 VCO feedback integer divider bit0 | R/W | | | 0 |

## SMBus Table Byte 5: PLL3 Loop Filter Setting and N Divider 10:8

| Byte 05h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|------|------------------|------|---|---|-----|
| Bit 7 | PLL3_R100K | PLL3 Loop filter resister 100kΩ | R/W | bypass | plus 100kΩ | 0 |
| Bit 6 | PLL3_R50K | PLL3 Loop filter resister 50kΩ | R/W | bypass | plus 50kΩ | 0 |
| Bit 5 | PLL3_R25K | PLL3 Loop filter resister 25kΩ | R/W | bypass | plus 25kΩ | 0 |
| Bit 4 | PLL3_R12.5K | PLL3 Loop filter resister 12.5kΩ | R/W | bypass | plus 12.5kΩ | 1 |
| Bit 3 | PLL3_R6K | PLL3 Loop filter resister 6kΩ | R/W | bypass | only 6kΩ applied | 0 |
| Bit 2 | PLL3 N_DIV[10] | PLL3 VCO feedback integer divider bit10 | R/W | | | 0 |
| Bit 1 | PLL3 N_DIV[9] | PLL3 VCO feedback integer divider bit9 | R/W | 12–2048, default VCO setting is 480MHz | | 0 |
| Bit 0 | PLL3 N_DIV[8] | PLL3 VCO feedback integer divider bit8 | R/W | | | 1 |

## SMBus Table Byte 6: PLL3 Charge Pump Control

| Byte 06h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUTDIV 3 Source | Output divider 3 source clock selection | R/W | PLL2 | DIV4seed | 0 |
| Bit 6 | PLL3_CP_8X | PLL3 charge pump control | R/W | — | x8 | 1 |
| Bit 5 | PLL3_CP_4X | PLL3 charge pump control | R/W | — | x4 | 1 |
| Bit 4 | PLL3_CP_2X | PLL3 charge pump control | R/W | — | x2 | 0 |
| Bit 3 | PLL3_CP_1X | PLL3 charge pump control | R/W | — | x1 | 1 |
| Bit 2 | PLL3_CP_/24 | PLL3 charge pump control | R/W | — | /24 | 1 |
| Bit 1 | PLL3_CP_/3 | PLL3 charge pump control | R/W | — | /3 | 0 |
| Bit 0 | PLL3_SIREF | PLL3 SiRef current selection | R/W | 10µA | 20µA | 0 |

Note: Formula: (iRef (10µA) × (1+SiRef) × (1 × 1X + 2 × 2X + 4 × 4X + 8 × 8X + 16 × 16X)) / ((24 × /24) + (3 × /3))

## SMBus Table Byte 7: PLL1 Control and OUTDIV5 Divider

| Byte 07h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL1_MDIV_Doubler | PLL1 reference clock doubler | R/W | disable | enable | 0 |
| Bit 6 | PLL1_SIREF | PLL1 SiRef current selection | R/W | 10.8µA | 21.6µA | 0 |
| Bit 5 | PLL1_EN_CH2 | PLL1 output Channel 2 control | R/W | disable | enable | 1 |
| Bit 4 | PLL1_EN_3rdpole | PLL1 3rd pole control | R/W | disable | enable | 0 |
| Bit 3 | OUTDIV5[3] | Output divider5 control bit 3 | R/W | DIV5[3:2] = 1,2,4,5; DIV5[1:0] = 1,3,5,10; Default Divider = 1 × 10 = 10 | | 0 |
| Bit 2 | OUTDIV5[2] | Output divider5 control bit 2 | R/W | | | 0 |
| Bit 1 | OUTDIV5[1] | Output divider5 control bit 1 | R/W | | | 1 |
| Bit 0 | OUTDIV5[0] | Output divider5 control bit 0 | R/W | | | 1 |

## SMBus Table Byte 8: PLL1 M Divider

| Byte 08h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL1_MDIV1 | PLL3 VCO reference clock divider 1 | R/W | disable M DIV1 | bypass divider (/1) | 0 |
| Bit 6 | PLL1_MDIV2 | PLL3 VCO reference clock divider 2 | R/W | disable M DIV2 | bypass divider (/2) | 0 |
| Bit 5 | PLL1 M_DIV[5] | PLL1 reference clock divider control bit 5 | R/W | 3–64, default is 26 | | 0 |
| Bit 4 | PLL1 M_DIV[4] | PLL1 reference clock divider control bit 4 | R/W | | | 1 |
| Bit 3 | PLL1 M_DIV[3] | PLL1 reference clock divider control bit 3 | R/W | | | 1 |
| Bit 2 | PLL1 M_DIV[2] | PLL1 reference clock divider control bit 2 | R/W | | | 0 |
| Bit 1 | PLL1 M_DIV[1] | PLL1 reference clock divider control bit 1 | R/W | | | 1 |
| Bit 0 | PLL1 M_DIV[0] | PLL1 reference clock divider control bit 0 | R/W | | | 0 |

## SMBus Table Byte 9: PLL1 VCO N Divider

| Byte 09h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL1 N_DIV[7] | PLL1 VCO feedback divider control bit 7 | R/W | | | 0 |
| Bit 6 | PLL1 N_DIV[6] | PLL1 VCO feedback divider control bit 6 | R/W | | | 1 |
| Bit 5 | PLL1 N_DIV[5] | PLL1 VCO feedback divider control bit 5 | R/W | | | 0 |
| Bit 4 | PLL1 N_DIV[4] | PLL1 VCO feedback divider control bit 4 | R/W | 12–2048, default is 600 | | 1 |
| Bit 3 | PLL1 N_DIV[3] | PLL1 VCO feedback divider control bit 3 | R/W | | | 1 |
| Bit 2 | PLL1 N_DIV[2] | PLL1 VCO feedback divider control bit 2 | R/W | | | 0 |
| Bit 1 | PLL1 N_DIV[1] | PLL1 VCO feedback divider control bit 1 | R/W | | | 0 |
| Bit 0 | PLL1 N_DIV[0] | PLL1 VCO feedback divider control bit 0 | R/W | | | 0 |

## SMBus Table Byte 10: PLL Loop Filter and N Divider

| Byte 0Ah | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL1_R100K | PLL1 loop filter resister 100kΩ | R/W | bypass | plus 100kΩ | 1 |
| Bit 6 | PLL1_R50K | PLL1 loop filter resister 50kΩ | R/W | bypass | plus 50kΩ | 0 |
| Bit 5 | PLL1_R25K | PLL1 loop filter resister 25kΩ | R/W | bypass | plus 25kΩ | 1 |
| Bit 4 | PLL1_R12.5K | PLL1 loop filter resister 12.5kΩ | R/W | bypass | plus 12.5kΩ | 1 |
| Bit 3 | PLL1_R1.0K | PLL1 loop filter resister 1kΩ | R/W | bypass | only 1.0kΩ applied | 0 |
| Bit 2 | PLL1 N_DIV[10] | PLL1 VCO feedback integer divider bit 10 | R/W | | | 0 |
| Bit 1 | PLL1 N_DIV[9] | PLL1 VCO feedback integer divider bit 9 | R/W | 12–2048, default is 600 | | 1 |
| Bit 0 | PLL1 N_DIV[8] | PLL1 VCO feedback integer divider bit 8 | R/W | | | 0 |

## SMBus Table Byte 11: PLL1 Charge Pump

| Byte 0Bh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL1_CP_32X | PLL1 charge pump control | R/W | — | x32 | 0 |
| Bit 6 | PLL1_CP_16X | PLL1 charge pump control | R/W | — | x16 | 0 |
| Bit 5 | PLL1_CP_8X | PLL1 charge pump control | R/W | — | x8 | 0 |
| Bit 4 | PLL1_CP_4X | PLL1 charge pump control | R/W | — | x4 | 0 |
| Bit 3 | PLL1_CP_2X | PLL1 charge pump control | R/W | — | x2 | 0 |
| Bit 2 | PLL1_CP_1X | PLL1 charge pump control | R/W | — | x1 | 1 |
| Bit 1 | PLL1_CP_/24 | PLL1 charge pump control | R/W | — | /24 | 1 |
| Bit 0 | PLL1_CP_/3 | PLL1 charge pump control | R/W | — | /3 | 0 |

## SMBus Table Byte 12: PLL1 Spread Spectrum Control

| Byte 0Ch | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL1_SS_REFDIV23 | PLL1 spread spectrum control- Ref divider 23 | R/W | — | — | 0 |
| Bit 6 | PLL1_SS_REFDIV[6] | PLL1 spread spectrum control- Ref divider 6 | R/W | — | — | 0 |
| Bit 5 | PLL1_SS_REFDIV[5] | PLL1 spread spectrum control- Ref divider 5 | R/W | — | — | 0 |
| Bit 4 | PLL1_SS_REFDIV[4] | PLL1 spread spectrum control- Ref divider 4 | R/W | — | — | 0 |
| Bit 3 | PLL1_SS_REFDIV[3] | PLL1 spread spectrum control- Ref divider 3 | R/W | — | — | 0 |
| Bit 2 | PLL1_SS_REFDIV[2] | PLL1 spread spectrum control- Ref divider 2 | R/W | — | — | 0 |
| Bit 1 | PLL1_SS_REFDIV[1] | PLL1 spread spectrum control- Ref divider 1 | R/W | — | — | 0 |
| Bit 0 | PLL1_SS_REFDIV[0] | PLL1 spread spectrum control- Ref divider 0 | R/W | — | — | 0 |

## SMBus Table Byte 13: PLL1 Spread Spectrum Control

| Byte 0Dh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL1_SS_FBDIV[7] | PLL1 spread spectrum - feedback divider 7 | R/W | — | — | 0 |
| Bit 6 | PLL1_SS_FBDIV[6] | PLL1 spread spectrum - feedback divider 6 | R/W | — | — | 0 |
| Bit 5 | PLL1_SS_FBDIV[5] | PLL1 spread spectrum - feedback divider 5 | R/W | — | — | 0 |
| Bit 4 | PLL1_SS_FBDIV[4] | PLL1 spread spectrum - feedback divider 4 | R/W | — | — | 0 |
| Bit 3 | PLL1_SS_FBDIV[3] | PLL1 spread spectrum - feedback divider 3 | R/W | — | — | 0 |
| Bit 2 | PLL1_SS_FBDIV[2] | PLL1 spread spectrum - feedback divider 2 | R/W | — | — | 0 |
| Bit 1 | PLL1_SS_FBDIV[1] | PLL1 spread spectrum - feedback divider 1 | R/W | — | — | 0 |
| Bit 0 | PLL1_SS_FBDIV[0] | PLL1 spread spectrum - feedback divider 0 | R/W | — | — | 0 |

## SMBus Table Byte 14: PLL1 Spread Spectrum Control

| Byte 0Eh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL1_SS_FBDIV[15] | PLL1 spread spectrum - feedback divider 15 | R/W | — | — | 0 |
| Bit 6 | PLL1_SS_FBDIV[14] | PLL1 spread spectrum - feedback divider 14 | R/W | — | — | 0 |
| Bit 5 | PLL1_SS_FBDIV[13] | PLL1 spread spectrum - feedback divider 13 | R/W | — | — | 0 |
| Bit 4 | PLL1_SS_FBDIV[12] | PLL1 spread spectrum - feedback divider 12 | R/W | — | — | 0 |
| Bit 3 | PLL1_SS_FBDIV[11] | PLL1 spread spectrum - feedback divider 11 | R/W | — | — | 0 |
| Bit 2 | PLL1_SS_FBDIV[10] | PLL1 spread spectrum - feedback divider 10 | R/W | — | — | 0 |
| Bit 1 | PLL1_SS_FBDIV[09] | PLL1 spread spectrum - feedback divider 9 | R/W | — | — | 0 |
| Bit 0 | PLL1_SS_FBDIV[08] | PLL1 spread spectrum - feedback divider 8 | R/W | — | — | 0 |

**SMBus Table Byte 15: Output Divider 1 Control**

| Byte 0Fh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUTDIV1[3] | Output divider1 control bit 3 | R/W | | | 0 |
| Bit 6 | OUTDIV1[2] | Output divider1 control bit 2 | R/W | DIV1[3:2]=1,2,4,8; DIV1[1:0]=1,4,5,6; Default divider = 1x1=1 | | 0 |
| Bit 5 | OUTDIV1[1] | Output divider1 control bit 1 | R/W | | | 0 |
| Bit 4 | OUTDIV1[0] | Output divider1 control bit 0 | R/W | | | 0 |
| Bit 3 | OUTDIV2[3] | Output divider2 control bit 3 | R/W | | | 0 |
| Bit 2 | OUTDIV2[2] | Output divider2 control bit 2 | R/W | DIV2[3:2]=1,2,4,5; DIV2[1:0]=1,3,5,10; Default divider = 1x10=10 | | 0 |
| Bit 1 | OUTDIV2[1] | Output divider2 control bit 1 | R/W | | | 1 |
| Bit 0 | OUTDIV2[0] | Output divider2 control bit 0 | R/W | | | 1 |

**SMBus Table Byte 16: PLL2 Integer Feedback Divider**

| Byte 10h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | | Reserved | R/W | — | — | 0 |
| Bit 6 | | Reserved | R/W | — | — | 0 |
| Bit 5 | | Reserved | R/W | — | — | 0 |
| Bit 4 | | Reserved | R/W | — | — | 0 |
| Bit 3 | | Reserved | R/W | — | — | 0 |
| Bit 2 | PLL2_FB_INT[10] | PLL2 feedback integer divider 10 | R/W | — | — | 0 |
| Bit 1 | PLL2_FB_INT[9] | PLL2 feedback integer divider 9 | R/W | — | — | 0 |
| Bit 0 | PLL2_FB_INT[8] | PLL2 feedback integer divider 8 | R/W | — | — | 0 |

**SMBus Table Byte 17: PLL2 Integer Feedback Divider**

| Byte 11h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL2_FB_INT_DIV[7] | PLL2 feedback integer divider 7 | R/W | — | — | 0 |
| Bit 6 | PLL2_FB_INT_DIV[6] | PLL2 feedback integer divider 6 | R/W | — | — | 0 |
| Bit 5 | PLL2_FB_INT_DIV[5] | PLL2 feedback integer divider 5 | R/W | — | — | 1 |
| Bit 4 | PLL2_FB_INT_DIV[4] | PLL2 feedback integer divider 4 | R/W | — | — | 1 |
| Bit 3 | PLL2_FB_INT_DIV[3] | PLL2 feedback integer divider 3 | R/W | — | — | 1 |
| Bit 2 | PLL2_FB_INT_DIV[2] | PLL2 feedback integer divider 2 | R/W | — | — | 1 |
| Bit 1 | PLL2_FB_INT_DIV[1] | PLL2 feedback integer divider 1 | R/W | — | — | 0 |
| Bit 0 | PLL2_FB_INT_DIV[0] | PLL2 feedback integer divider 0 | R/W | — | — | 0 |

**SMBus Table Byte 18: PLL2 Fractional Feedback Divider**

| Byte 12h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL2_FB_FRC_DIV[7] | PLL2 feedback fractional divider 7 | R/W | — | — | 0 |
| Bit 6 | PLL2_FB_FRC_DIV[6] | PLL2 feedback fractional divider 6 | R/W | — | — | 0 |
| Bit 5 | PLL2_FB_FRC_DIV[5] | PLL2 feedback fractional divider 5 | R/W | — | — | 0 |
| Bit 4 | PLL2_FB_FRC_DIV[4] | PLL2 feedback fractional divider 4 | R/W | — | — | 0 |
| Bit 3 | PLL2_FB_FRC_DIV[3] | PLL2 feedback fractional divider 3 | R/W | — | — | 0 |
| Bit 2 | PLL2_FB_FRC_DIV[2] | PLL2 feedback fractional divider 2 | R/W | — | — | 0 |
| Bit 1 | PLL2_FB_FRC_DIV[1] | PLL2 feedback fractional divider 1 | R/W | — | — | 0 |
| Bit 0 | PLL2_FB_FRC_DIV[0] | PLL2 feedback fractional divider 0 | R/W | — | — | 0 |

**SMBus Table Byte 19: PLL2 Fractional Feedback Divider**

| Byte 13h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL2_FB_FRC_DIV[15] | PLL2 feedback fractional divider 15 | R/W | — | — | 0 |
| Bit 6 | PLL2_FB_FRC_DIV[14] | PLL2 feedback fractional divider 14 | R/W | — | — | 0 |
| Bit 5 | PLL2_FB_FRC_DIV[13] | PLL2 feedback fractional divider 13 | R/W | — | — | 0 |
| Bit 4 | PLL2_FB_FRC_DIV[12] | PLL2 feedback fractional divider 12 | R/W | — | — | 0 |
| Bit 3 | PLL2_FB_FRC_DIV[11] | PLL2 feedback fractional divider 11 | R/W | — | — | 0 |
| Bit 2 | PLL2_FB_FRC_DIV[10] | PLL2 feedback fractional divider 10 | R/W | — | — | 0 |
| Bit 1 | PLL2_FB_FRC_DIV[9] | PLL2 feedback fractional divider 9 | R/W | — | — | 0 |
| Bit 0 | PLL2_FB_FRC_DIV[8] | PLL2 feedback fractional divider 8 | R/W | — | — | 0 |

**SMBus Table Byte 20: PLL2 Spread Spectrum Control**

| Byte 14h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL2_STEP[7] | PLL2 spread step size control bit 7 | R/W | — | — | 0 |
| Bit 6 | PLL2_STEP[6] | PLL2 spread step size control bit 6 | R/W | — | — | 0 |
| Bit 5 | PLL2_STEP[5] | PLL2 spread step size control bit 5 | R/W | — | — | 0 |
| Bit 4 | PLL2_STEP[4] | PLL2 spread step size control bit 4 | R/W | — | — | 0 |
| Bit 3 | PLL2_STEP[3] | PLL2 spread step size control bit 3 | R/W | — | — | 0 |
| Bit 2 | PLL2_STEP[2] | PLL2 spread step size control bit 2 | R/W | — | — | 0 |
| Bit 1 | PLL2_STEP[1] | PLL2 spread step size control bit 1 | R/W | — | — | 0 |
| Bit 0 | PLL2_STEP[0] | PLL2 spread step size control bit 0 | R/W | — | — | 0 |

**SMBus Table Byte 21: PLL2 Spread Spectrum Control**

| Byte 15h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL2_STEP[15] | PLL2 spread step size control bit 15 | R/W | — | — | 0 |
| Bit 6 | PLL2_STEP[14] | PLL2 spread step size control bit 14 | R/W | — | — | 0 |
| Bit 5 | PLL2_STEP[13] | PLL2 spread step size control bit 13 | R/W | — | — | 0 |
| Bit 4 | PLL2_STEP[12] | PLL2 spread step size control bit 12 | R/W | — | — | 0 |
| Bit 3 | PLL2_STEP[11] | PLL2 spread step size control bit 11 | R/W | — | — | 0 |
| Bit 2 | PLL2_STEP[10] | PLL2 spread step size control bit 10 | R/W | — | — | 0 |
| Bit 1 | PLL2_STEP[9] | PLL2 spread step size control bit 9 | R/W | — | — | 0 |
| Bit 0 | PLL2_STEP[8] | PLL2 spread step size control bit 8 | R/W | — | — | 0 |

**SMBus Table Byte 22: PLL2 Spread Spectrum Control**

| Byte 16h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL2_STEP_DELTA[7] | PLL2 spread step size control delta bit 7 | R/W | — | — | 0 |
| Bit 6 | PLL2_STEP_DELTA[6] | PLL2 spread step size control delta bit 6 | R/W | — | — | 0 |
| Bit 5 | PLL2_STEP_DELTA[5] | PLL2 spread step size control delta bit 5 | R/W | — | — | 0 |
| Bit 4 | PLL2_STEP_DELTA[4] | PLL2 spread step size control delta bit 4 | R/W | — | — | 0 |
| Bit 3 | PLL2_STEP_DELTA[3] | PLL2 spread step size control delta bit 3 | R/W | — | — | 0 |
| Bit 2 | PLL2_STEP_DELTA[2] | PLL2 spread step size control delta bit 2 | R/W | — | — | 0 |
| Bit 1 | PLL2_STEP_DELTA[1] | PLL2 spread step size control delta bit 1 | R/W | — | — | 0 |
| Bit 0 | PLL2_STEP_DELTA[0] | PLL2 spared step size control delta bit 0 | R/W | — | — | 0 |

**SMBus Table Byte 23: PLL2 Period Control**

| Byte 17h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL2_PERIOD[7] | PLL2 period control bit 7 | R/W | — | — | 0 |
| Bit 6 | PLL2_PERIOD[6] | PLL2 period control bit 6 | R/W | — | — | 0 |
| Bit 5 | PLL2_PERIOD[5] | PLL2 period control bit 5 | R/W | — | — | 0 |
| Bit 4 | PLL2_PERIOD[4] | PLL2 period control bit 4 | R/W | — | — | 0 |
| Bit 3 | PLL2_PERIOD[3] | PLL2 period control bit 3 | R/W | — | — | 0 |
| Bit 2 | PLL2_PERIOD[2] | PLL2 period control bit 2 | R/W | — | — | 0 |
| Bit 1 | PLL2_PERIOD[1] | PLL2 period control bit 1 | R/W | — | — | 0 |
| Bit 0 | PLL2_PERIOD[0] | PLL2 period control bit 0 | R/W | — | — | 0 |

## SMBus Table Byte 24: PLL2 Control Register

| Byte 18h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL2_PERIOD[9] | PLL2 period control bit 9 | R/W | — | — | 0 |
| Bit 6 | PLL2_PERIOD[8] | PLL2 period control bit 8 | R/W | — | — | 0 |
| Bit 5 | PLL2_SSEN | PLL2 spread spectrum enable | R/W | disable | enable | 0 |
| Bit 4 | PLL2_R100K | PLL2 Loop filter resister 100kΩ | R/W | bypass | plus 100kΩ | 0 |
| Bit 3 | PLL2_R50K | PLL2 Loop filter resister 50kΩ | R/W | bypass | plus 50kΩ | 1 |
| Bit 2 | PLL2_R25K | PLL2 Loop filter resister 25kΩ | R/W | bypass | plus 25kΩ | 1 |
| Bit 1 | PLL2_R12.5K | PLL2 Loop filter resister 12.5kΩ | R/W | bypass | plus 12.5kΩ | 1 |
| Bit 0 | PLL2_R6K | PLL2 Loop filter resister 6kΩ | R/W | bypass | only 6kΩ applied | 0 |

## SMBus Table Byte 25: PLL2 Charge Pump Control

| Byte 19h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL2_CP_16X | PLL2 charge pump control | R/W | — | x16 | 0 |
| Bit 6 | PLL2_CP_8X | PLL2 charge pump control | R/W | — | x8 | 0 |
| Bit 5 | PLL2_CP_4X | PLL2 charge pump control | R/W | — | x4 | 0 |
| Bit 4 | PLL2_CP_2X | PLL2 charge pump control | R/W | — | x2 | 1 |
| Bit 3 | PLL2_CP_1X | PLL2 charge pump control | R/W | — | x1 | 0 |
| Bit 2 | PLL2_CP_/24 | PLL2 charge pump control | R/W | — | /24 | 1 |
| Bit 1 | PLL2_CP_/3 | PLL2 charge pump control | R/W | — | /3 | 0 |
| Bit 0 | PLL2_SIREF | PLL2 SiRef current selection | R/W | 10µA | 20µA | 0 |

## SMBus Table Byte 26: PLL2 M Divider Setting

| Byte 1Ah | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL2_MDIV_Doubler | PLL2 reference divider - doubler | R/W | disable | enable | 0 |
| Bit 6 | PLL2_MDIV1 | PLL2 reference divider 1 | R/W | disable M DIV1 | bypadd divider (/1) | 0 |
| Bit 5 | PLL2_MDIV2 | PLL2 reference divider 2 | R/W | disable M DIV2 | bypadd divider (/2) | 0 |
| Bit 4 | PLL2_MDIV[4] | PLL2 reference divider control bit 4 | R/W | | | 1 |
| Bit 3 | PLL2_MDIV[3] | PLL2 reference divider control bit 3 | R/W | | | 1 |
| Bit 2 | PLL2_MDIV[2] | PLL2 reference divider control bit 2 | R/W | 3–64, default is 26 | | 0 |
| Bit 1 | PLL2_MDIV[1] | PLL2 reference divider control bit 1 | R/W | | | 1 |
| Bit 0 | PLL2_MDIV[0] | PLL2 reference divider control bit 0 | R/W | | | 0 |

**SMBus Table Byte 27: Output Divider 4**

| Byte 1Bh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUTDIV3[3] | Out divider 4 control bit 7 | R/W | | | 0 |
| Bit 6 | OUTDIV3[2] | Out divider 4 control bit 6 | R/W | DIV3[3:2]=1,2,4,5; DIV3[1:0]=1,3,5,10; Default divider = 1x5=5 | | 0 |
| Bit 5 | OUTDIV3[1] | Out divider 4 control bit 5 | R/W | | | 1 |
| Bit 4 | OUTDIV3[0] | Out divider 4 control bit 4 | R/W | | | 0 |
| Bit 3 | OUTDIV4[3] | Out divider 4 control bit 3 | R/W | | | 0 |
| Bit 2 | OUTDIV4[2] | Out divider 4 control bit 2 | R/W | DIV4[3:2]=1,2,4,8; DIV4[1:0]=1,3,5,10; Default divider = 1x10=10 | | 0 |
| Bit 1 | OUTDIV4[1] | Out divider 4 control bit 1 | R/W | | | 1 |
| Bit 0 | OUTDIV4[0] | Out divider 4 control bit 0 | R/W | | | 1 |

**SMBus Table Byte 28: PLL Operation Control Register**

| Byte 1Ch | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PLL2_HRS_EN | PLL2 spread high resolution selection enable | R/W | normal | enable (shift 4 bits) | 0 |
| Bit 6 | PLL2_refin_sel | PLL2 reference clock source select | R/W | Xtal | DIV2 | 0 |
| Bit 5 | PLL3_PDB | PLL3 power down | R/W | power down | running | 0 |
| Bit 4 | PLL3_LCKBYPSSB | PLL3 lock bypass | R/W | bypass lock | lock | 0 |
| Bit 3 | PLL2_PDB | PLL2 power down | R/W | power down | running | 1 |
| Bit 2 | PLL2_LCKBYPSSB | PLL2 lock bypass | R/W | bypass lock | lock | 1 |
| Bit 1 | PLL1_PDB | PLL1 power down | R/W | power down | running | 0 |
| Bit 0 | PLL1_LCKBYPSSB | PLL1 lock bypass | R/W | bypass lock | lock | 0 |

**SMBus Table Byte 29: Output Control**

| Byte 1Dh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | | Reserved | R/W | — | — | 0 |
| Bit 6 | | Reserved | R/W | — | — | 0 |
| Bit 5 | | Reserved | R/W | — | — | 1 |
| Bit 4 | | Reserved | R/W | — | — | 1 |
| Bit 3 | | Reserved | R/W | — | — | 0 |
| Bit 2 | | Reserved | R/W | — | — | 0 |
| Bit 1 | | Reserved | R/W | — | — | 0 |
| Bit 0 | | Reserved | R/W | — | — | 0 |

## SMBus Table Byte 30: OE and DFC Control

| Byte 1Eh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUT1_EN | OUT1 output enable control | R/W | disable | enable | 1 |
| Bit 6 | OE1_fun_sel[1] | OE1 pin function selection bit 1 | R/W | 11:DFC0    10: OUT1_PPS | | 0 |
| Bit 5 | OE1_fun_sel[0] | OE1 pin function selection bit 0 | R/W | 01: PD#    00: OUT1 OE | | 0 |
| Bit 4 | OUT3_EN | OUT3 output enable control | R/W | disable | enable | 1 |
| Bit 3 | Reserved | | R/W | — | — | 0 |
| Bit 2 | Reserved | | R/W | — | — | 0 |
| Bit 1 | DFC_SW_Sel[1] | DFC frequency select bit 1 | R/W | 00: N0 01: N1 10:N2 11:N3 | | 0 |
| Bit 0 | DFC_SW_Sel[0] | DFC frequency select bit 0 | R/W | | | 0 |

## SMBus Table Byte 31: Control Register

| Byte 1Fh | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUT2 free run_b | OUT2 free run_b | R/W | freerun | stoppable | 1 |
| Bit 6 | Reserved | | R/W | — | — | 0 |
| Bit 5 | Reserved | | R/W | — | — | 0 |
| Bit 4 | Reserved | | R/W | — | — | 0 |
| Bit 3 | Reserved | | R/W | — | — | 0 |
| Bit 2 | PLL2_3rd_EN_CFG | PLL2 3rd order control | R/W | 1st order | 3rd order | 1 |
| Bit 1 | OUTDIV5 source | OUTDIV5 source | R/W | PLL3 | DIV4seed | 0 |
| Bit 0 | PLL2_EN_3rdpole | PLL2 3rd Pole control | R/W | disable | enable | 0 |

## SMBus Table Byte 32: Control Register

| Byte 20h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUT2_EN | OUT2 output enable control | R/W | disable | enable | 1 |
| Bit 6 | Reserved | | R/W | — | — | 0 |
| Bit 5 | Reserved | | R/W | — | — | 0 |
| Bit 4 | DFC_EN | DFC function control | R/W | disable | enable | 0 |
| Bit 3 | Reserved | | R/W | — | — | 0 |
| Bit 2 | Reserved | | R/W | — | — | 0 |
| Bit 1 | Reserved | | R/W | — | — | 0 |
| Bit 0 | Reserved | | R/W | — | — | 0 |

## SMBus Table Byte 33: OUT3 Control Register

| Byte 21h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUT3 free run_b | OUT3 free run_b | R/W | freerun | stoppable | 1 |
| Bit 6 | Reserved | | R/W | — | — | 0 |
| Bit 5 | Reserved | | R/W | — | — | 0 |
| Bit 4 | Reserved | | R/W | — | — | 0 |
| Bit 3 | Reserved | | R/W | — | — | 0 |
| Bit 2 | Reserved | | R/W | — | — | 0 |
| Bit 1 | Reserved | | R/W | — | — | 0 |
| Bit 0 | Reserved | | R/W | — | — | 0 |

## SMBus Table Byte 34: Control Register

| Byte 22h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | R/W | — | — | 1 |
| Bit 6 | Reserved | | R/W | — | — | 1 |
| Bit 5 | Reserved | | R/W | — | — | 1 |
| Bit 4 | Reserved | | R/W | — | — | 1 |
| Bit 3 | Reserved | | R/W | — | — | 0 |
| Bit 2 | Reserved | | R/W | — | — | 1 |
| Bit 1 | Reserved | | R/W | — | — | 0 |
| Bit 0 | Reserved | | R/W | — | — | 0 |

## SMBus Table Byte 35: Control Register

| Byte 23h | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | OUT3 muxsel1 | OUT3 muxsel1 | R/W | 00: DIV3   01: DIV5 10: DIV1 11: CLK_32K | | 1 |
| Bit 6 | OUT3 muxsel0 | OUT3 muxsel0 | R/W | | | 0 |
| Bit 5 | OUT2 muxsel1 | OUT2 muxsel1 | R/W | 00: DIV3   01: DIV5 10: DIV1 11: CLK_32K | | 0 |
| Bit 4 | OUT2 muxsel0 | OUT2 muxsel0 | R/W | | | 0 |
| Bit 3 | OUT1 muxsel1 | OUT1 muxsel1 | R/W | 00: DIV3   01: DIV5 10: DIV1 11: CLK_32K | | 1 |
| Bit 2 | OUT1 muxsel0 | OUT1 muxsel0 | R/W | | | 1 |
| Bit 1 | DIV1 muxsel1 | DIV1 muxsel1 | R/W | 00: PLL1   01: REF 1x: DIV4outseed | | 0 |
| Bit 0 | DIV1 muxsel0 | DIV1 muxsel0 | R/W | | | 1 |

**SMBus Table Byte 36: OUT1 and DIV4 Control**

| Byte 24h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|------|------------------|------|---|---|-----|
| Bit 7 | I2C_PDB | Chip power down control bit | R/W | power down | normal | 1 |
| Bit 6 | Ref_free_run | Reference clock output (OUT2/OUT3) | R/W | stop | freerun | 0 |
| Bit 5 | free_run_output_config | Clocks free run control | R/W | OUT2 freerun | OUT2/3 freerun | 0 |
| Bit 4 | Reserved | | R/W | — | — | 1 |
| Bit 3 | OUT1_Freerun_b | OUT1 free run_b | R/W | freerun | stoppable | 1 |
| Bit 2 | Enable OE2/3 | Enable OE2/OE3 function | R/W | Disable | Enable | 0 |
| Bit 1 | DIV4 muxsel1 | DIV4 muxsel1 | R/W | 00: PLL2_CH2   01: PLL3_CH2 10: DIV3seed 11: DIV5seed | | 1 |
| Bit 0 | DIV4 muxsel0 | DIV4 muxsel0 | R/W | | | 1 |

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 06/21/16 | JH |

PIN 1
ID CORNER

2.50 BSC  [A]

[B]

2.50 BSC

⌒ 0.10 C  2X

⌒ 0.10 C  2X

TOP VIEW

0.50±0.05

0.20±0.05  12          1

0.40 BSC

7          6

0.40±0.05

BOTTOM VIEW

// 0.10 C

0.90±0.10

⌒ 0.08 C

[C]

SIDE VIEW (ROTATE 90 Deg.)

NOTE:
1. Dimensioning and tolerancing conform to ASME Y14.5−2009.
2. All dimensions are in millimeters.

TOLERANCES
UNLESS SPECIFIED
DECIMAL        ANGULAR
X±  .1          ±1°
XX±  .05
XXX±  .030

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FAX: (408) 284−3572

| APPROVALS | | DATE | TITLE   ND/NDG12 PACKAGE OUTLINE |
|---|---|---|---|
| DRAWN | RAC | 6/21/16 | 2.50 x 2.50 mm BODY |
| CHECKED | | | 0.40 mm PITCH DFN |

| SIZE | DRAWING No. | | REV |
|---|---|---|---|
| C | PSC−4665 | | 00 |
| | DO NOT SCALE DRAWING | SHEET 1 OF 2 | |

Figure 7. NDG12 Package Drawing – page 2

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 06/21/16 | JH |

2.80

0.65

1          12

0.20

0.40

6          7

0.55          0.55
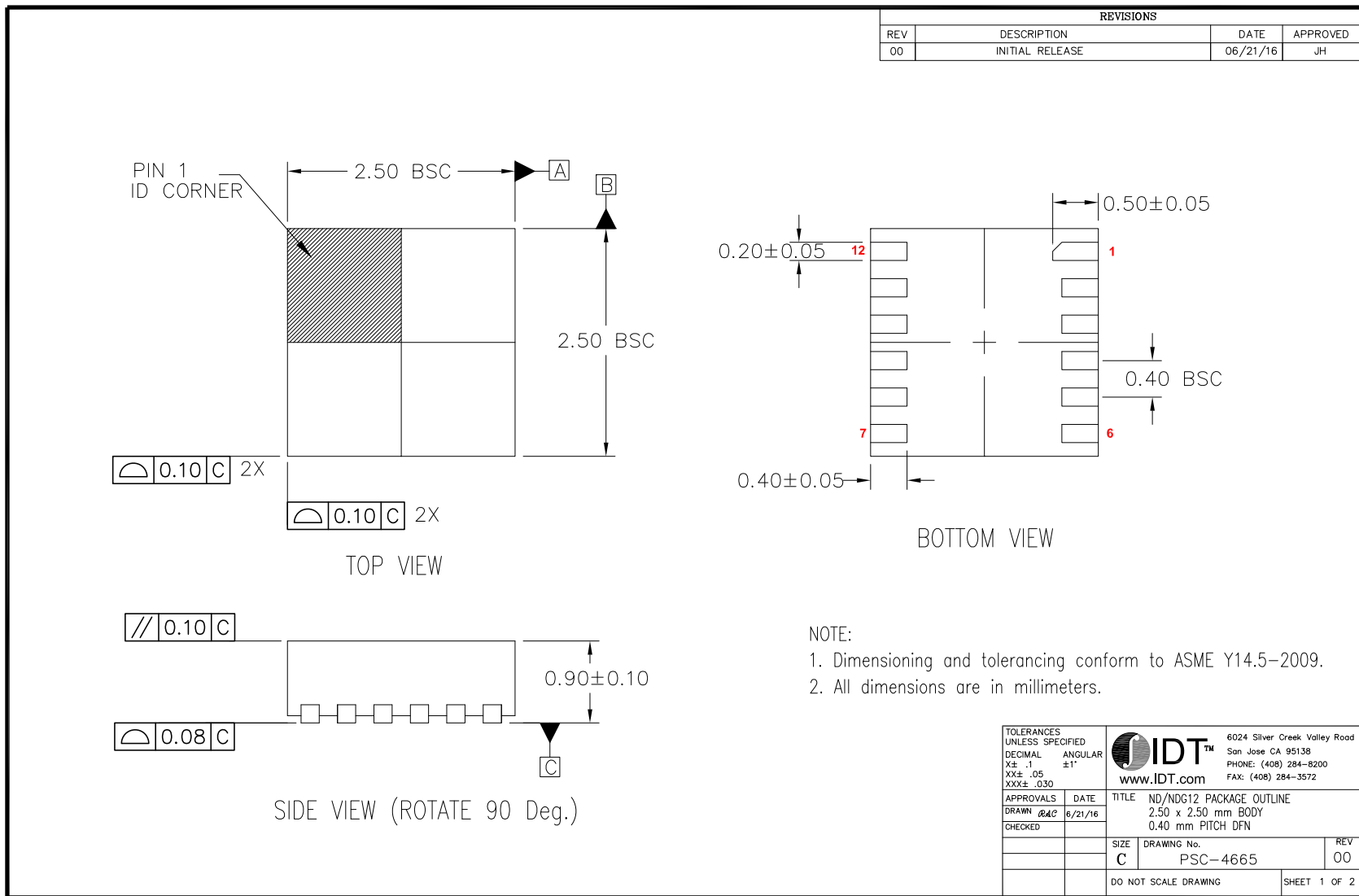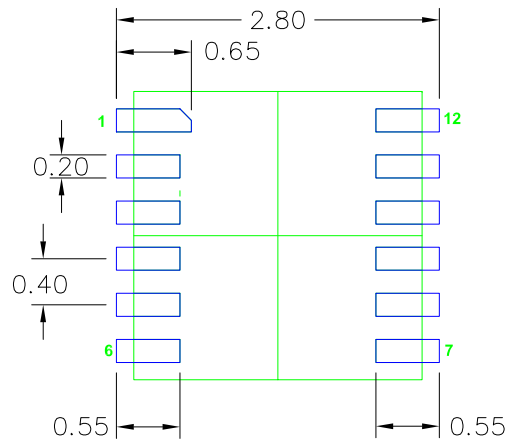
RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.

2. TOP DOWN VIEW. AS VIEWED ON PCB.

3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.

4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.

5. LAND PATTERN RECOMMENDATION PER IPC−7351B GENERIC REQUIREMENT
   FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

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|---|---|---|---|
| DECIMAL | ANGULAR | | |
| X± .1 | ±1° | | |
| XX± .05 | | | |
| XXX± .030 | | | |

| APPROVALS | DATE | TITLE ND/NDG12 PACKAGE OUTLINE 2.50 x 2.50 mm BODY 0.40 mm PITCH DFN | |
|---|---|---|---|
| DRAWN RAC | 6/21/16 | | |
| CHECKED | | | |
| | | SIZE C | DRAWING No. PSC−4665 | REV 00 |
| | | DO NOT SCALE DRAWING | SHEET 2 OF 2 |

## Ordering Information

| Orderable Part Number | Package | Shipping Packaging | Temperature |
|---|---|---|---|
| 5X2503-000NDGI | 2.5 × 2.5 mm, 0.4mm pitch 12-DFN | Cut Tape | -40° to +85°C |
| 5X2503-000NDGI8 | 2.5 × 2.5 mm, 0.4mm pitch 12-DFN | Reel | -40° to +85°C |

## Marking Diagram

```
X000
Y**
●
```
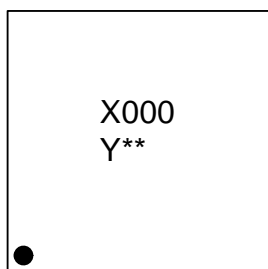
1. Line 1 is the truncated part number.

2. "000" denotes dash code.

3. "Y" is the last digit of the year the part was assembled.

4. "**" denotes sequential lot number.

## Revision History

| Revision Date | Description of Change |
|---|---|
| December 18, 2017 | Corrected bit setting in Byte 24h, bit 2 from "1" to "0". |
| November 17, 2017 | Updated register tables; Bytes 29, 30 and 32. |
| October 20, 2017 | Initial release. |

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