HIGH-SPEED 4K x 9DUAL-PORT STATIC RAM

7014S

Features:

- **True Dual-Ported memory cells which allow simultaneous reads of the same memory location**
- **High-speed access**
  - *Commercial: 12ns (max.)*
  - **Standard-power operation**
  - *IDT7014S*
    Active: 750mW (typ.)
- **Fully asynchronous operation from either port**
- **TTL-compatible; single 5V (±10%) power supply**
- **Available in 52-pin PLCC and a 64-pin TQFP**

Description:

The IDT7014 is a high-speed 4K x 9 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to high-speed applications which do not rely on BUSY signals to manage simultaneous access.

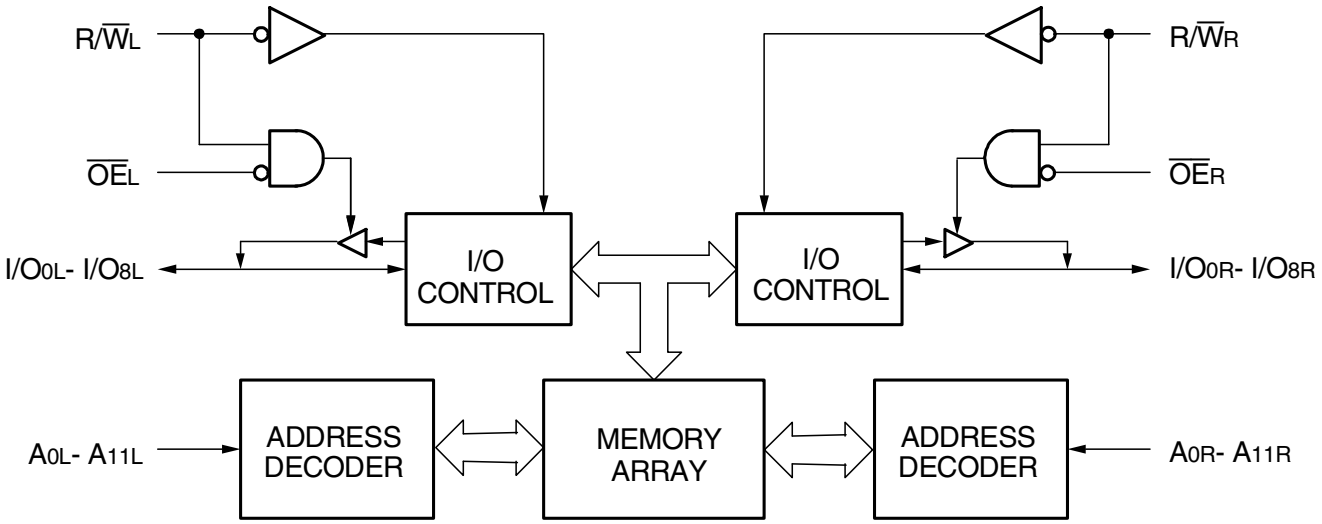
The IDT7014 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. See functional description.

The IDT7014 utilizes a 9-bit wide data path to allow for parity at the user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/ reception error checking.

Fabricated using a high-performance technology, these Dual-Ports typically operate on only 750mW of power at maximum access times as fast as 12ns.

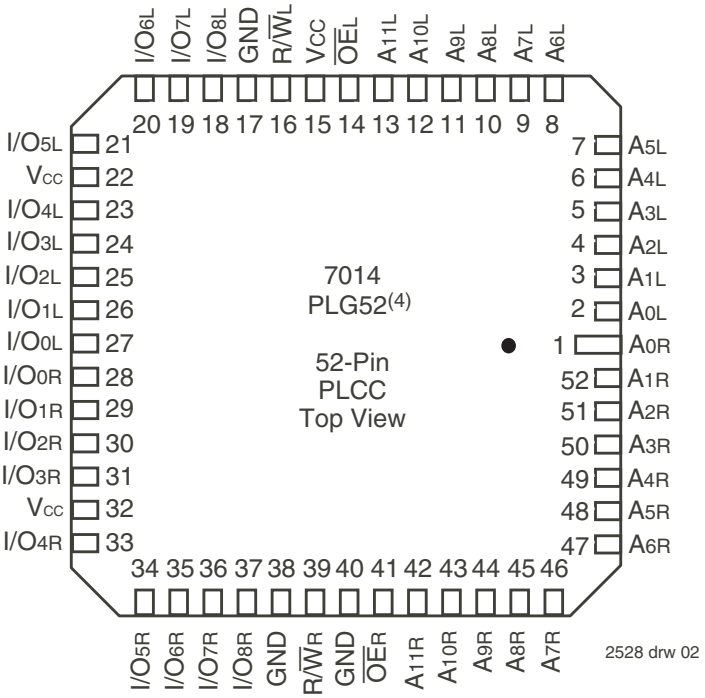
The IDT7014 is packaged in a 52-pin PLCC and a 64-pin thin quad flatpack, (TQFP).

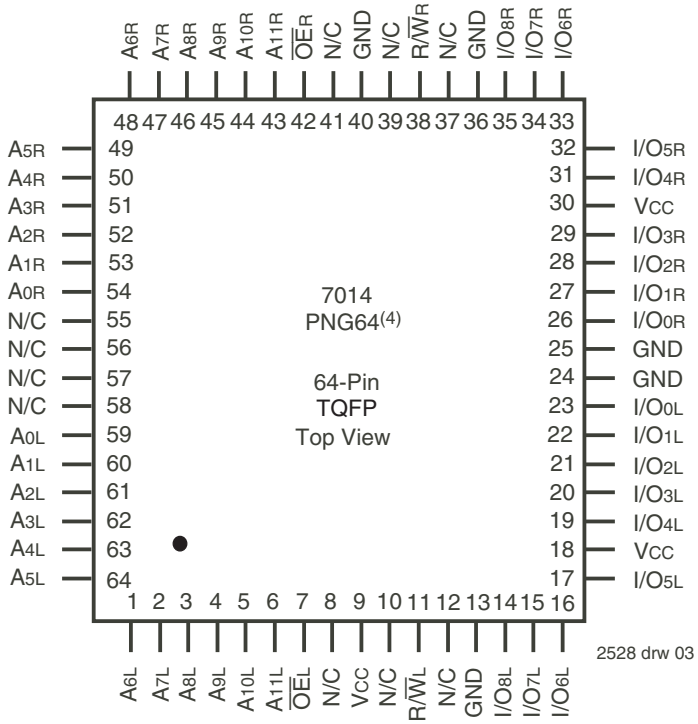
Functional Block Diagram



2528 drw 01

Pin Configuration[1,2,3]





NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. PLG52 package body is approximately .75 in x .75 in. x .17 in.
   PNG64 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V_{TERM}(2)	Terminal Voltage	-0.5 to +V_{CC}	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

2528 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 10%.

Maximum Operating Temperature and Supply Voltage(1,2)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2528 tbl 02

NOTES:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2528 tbl 03

NOTES:
1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7014S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

2528 tbl 04

NOTE:
1. At V_{CC} ≤ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version		7014S12 Com'l Only Typ.	7014S12 Com'l Only Max	7014S15 Com'l Only Typ.	7014S15 Com'l Only Max	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	Outputs Open f = f_{MAX}(1)	COM'L	S	160	250	160	250	mA
			IND	S	—	—	—	—	

2528 tbl 05a

Symbol	Parameter	Test Condition	Version		7014S20 Com'l & Ind Typ.	7014S20 Com'l & Ind Max	7014S25 Com'l Only Typ.	7014S25 Com'l Only Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	Outputs Open f = f_{MAX}(1)	COM'L	S	155	245	150	240	mA
			IND	S	155	260	—	—	

2528 tbl 05b

NOTES:
1. At f = fmax, address inputs are cycling at the maximum read cycle of 1/t_{RC} using the "AC Test Conditions" input levels of GND to 3V.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

2528 tbl 06

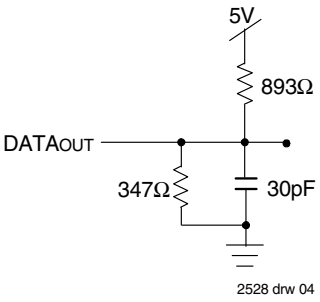


Figure 1. AC Output Test Load.

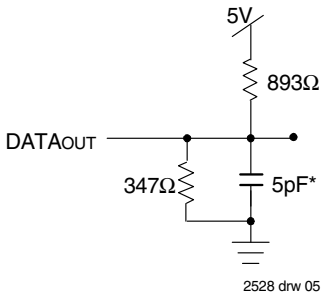


Figure 2. Output Test Load (for t_{HZ}, t_{WZ}, and t_{OW})
*Including scope and jig.

Capacitance(1)

(T_A = +25°C, f = 1.0MHz) TQFP Package Only

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

2528 tbl 07

NOTES:
1. This parameter is determined by device characteristics but is not production tested.
2. 3dv references the interpolated capacitance when the input and output signals with from 0V to 3V or from 3V to 0V.

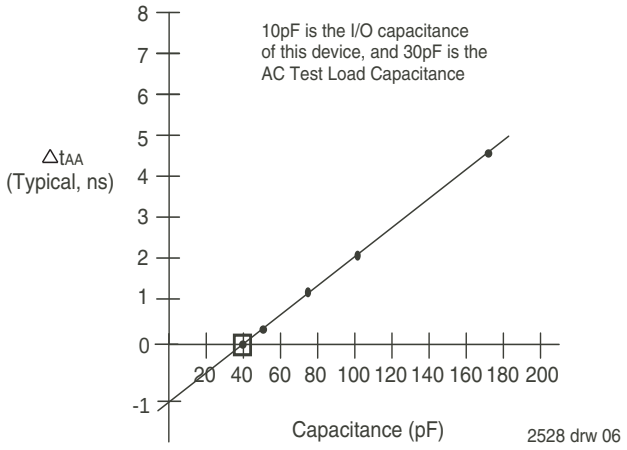


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

Symbol	Parameter	7014S12 Com'l Only		7014S15 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	12	—	15	—	ns
t_{AA}	Address Access Time	—	12	—	15	ns
t_{AOE}	Output Enable Access Time	—	8	—	8	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	7	—	7	ns

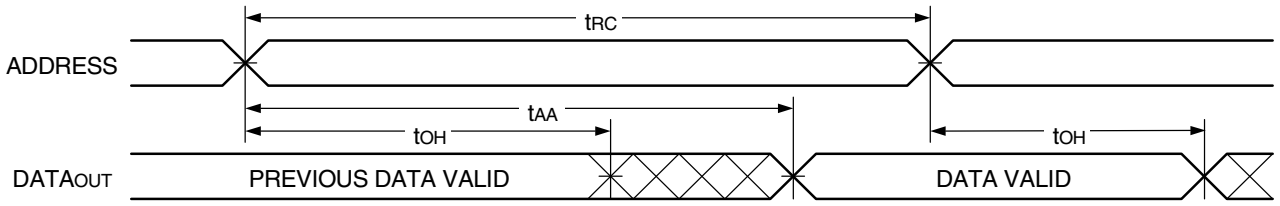
2528 tbl 08a

Symbol	Parameter	7014S20 Com'l & Ind		7014S25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	20	—	25	—	ns
t_{AA}	Address Access Time	—	20	—	25	ns
t_{AOE}	Output Enable Access Time	—	10	—	12	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	9	—	11	ns

2528 tbl 08b

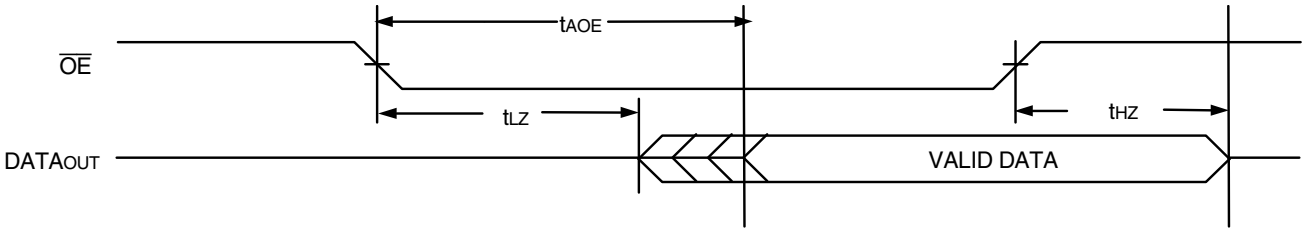
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is determined by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1, Either Side(1,2)



2528 drw 07

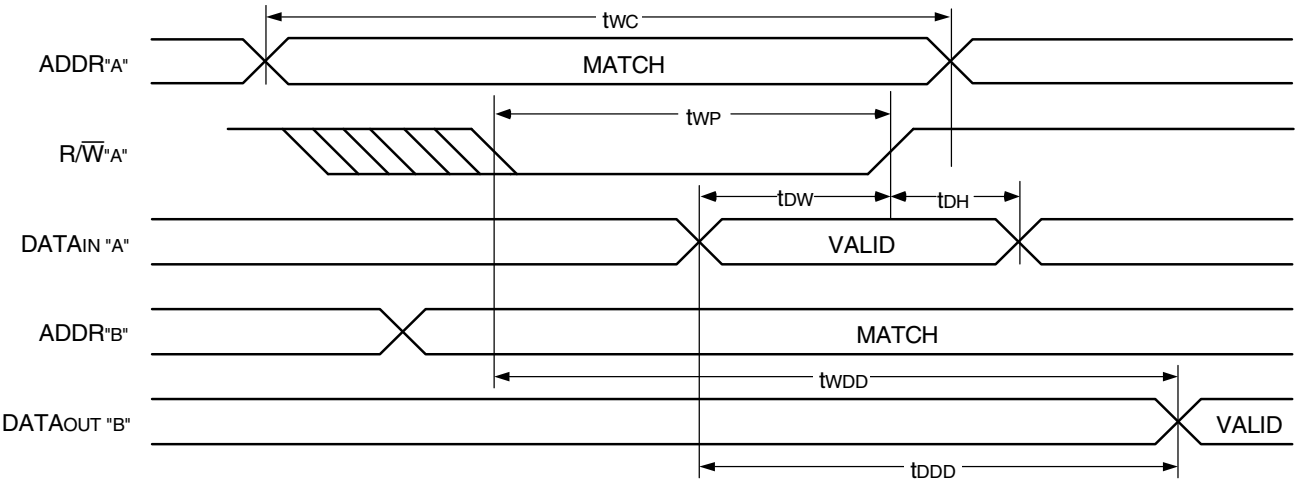
Timing Waveform of Read Cycle No. 2, Either Side(1, 3)



2528 drw 08

NOTES:
1. R/$\overline{W}$ = V_{IH} for Read Cycles.
2. $\overline{OE}$ = V_{IL}.
3. Addresses valid prior to $\overline{OE}$ transition LOW.

Timing Waveform of Write with Port-to-Port Read(1,2)



2528 drw 09

NOTES:
1. R/$\overline{W}$"B" = V_{IH}, read cycle pass through.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is opposite from port "A".

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

Symbol	Parameter	7014S12 Com'l Only		7014S15 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time	12	—	15	—	ns
t_{AW}	Address Valid to End-of-Write	10	—	14	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	10	—	12	—	ns
t_{WR}	Write Recovery Time	1	—	1	—	ns
t_{DW}	Data Valid to End-of-Write	8	—	10	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	7	—	7	ns
t_{DH}	Data Hold Time[3]	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	7	—	7	ns
t_{OW}	Output Active from End-of-Write[1,2,3]	0	—	0	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	25	—	30	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	22	—	25	ns

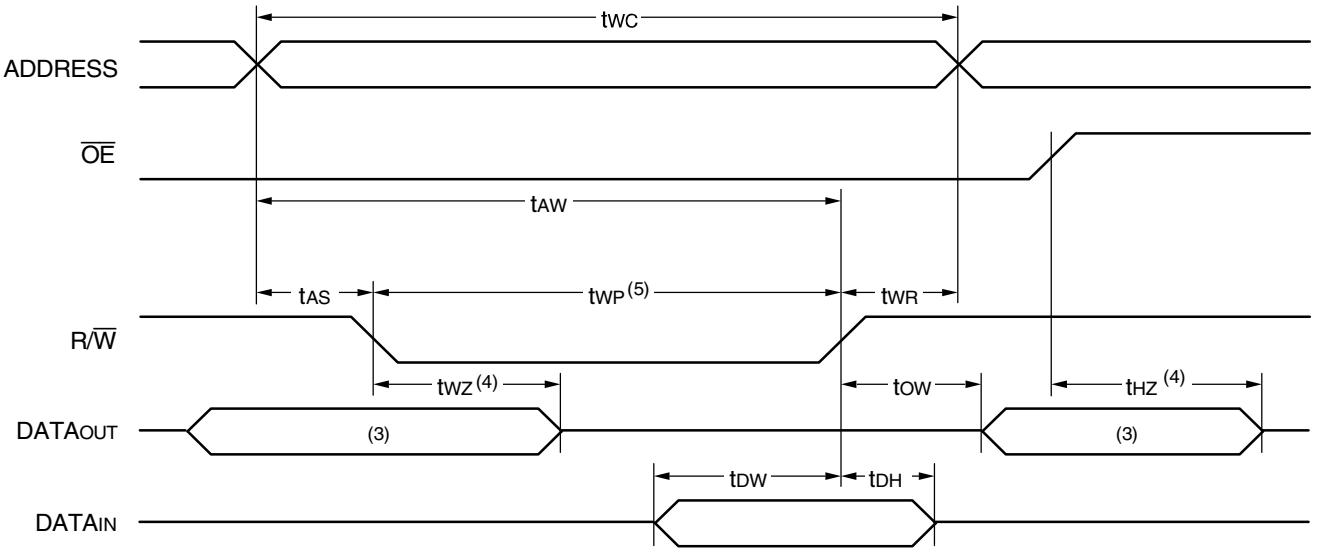
2528 tbl 09a

Symbol	Parameter	7014S20 Com'l & Ind		7014S25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time	20	—	25	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	ns
t_{WR}	Write Recovery Time	2	—	2	—	ns
t_{DW}	Data Valid to End-of-Write	12	—	15	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	9	—	11	ns
t_{DH}	Data Hold Time[3]	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	9	—	11	ns
t_{OW}	Output Active from End-of-Write[1,2,3]	0	—	0	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	40	—	45	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	30	—	35	ns

2528 tbl 09b

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write With Port-to-Port Read".

Timing Waveform of Write Cycle(1,2,3,4,5)



2528 drw 10

NOTES:
1. R/$\overline{W}$ must be HIGH during all address transitions.
2. t_{WR} is measured from R/$\overline{W}$ going HIGH to the end of write cycle.
3. During this period, the I/O pins are in the output state, and input signals must not be applied.
4. Transition is measured 0mV from the Low or High-impedance voltage with the Output Test Load (Figure 2).
5. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

Functional Description

The IDT7014 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. It lacks the chip enable feature of CMOS Dual Ports, thus it operates in active mode as soon as power is applied. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. The user application should avoid simultaneous write operations to the same memory location. There is no on-chip arbitration circuitry to resolve write priority and partial data from both ports may be written. READ/WRITE conditions are illustrated in Table 1.

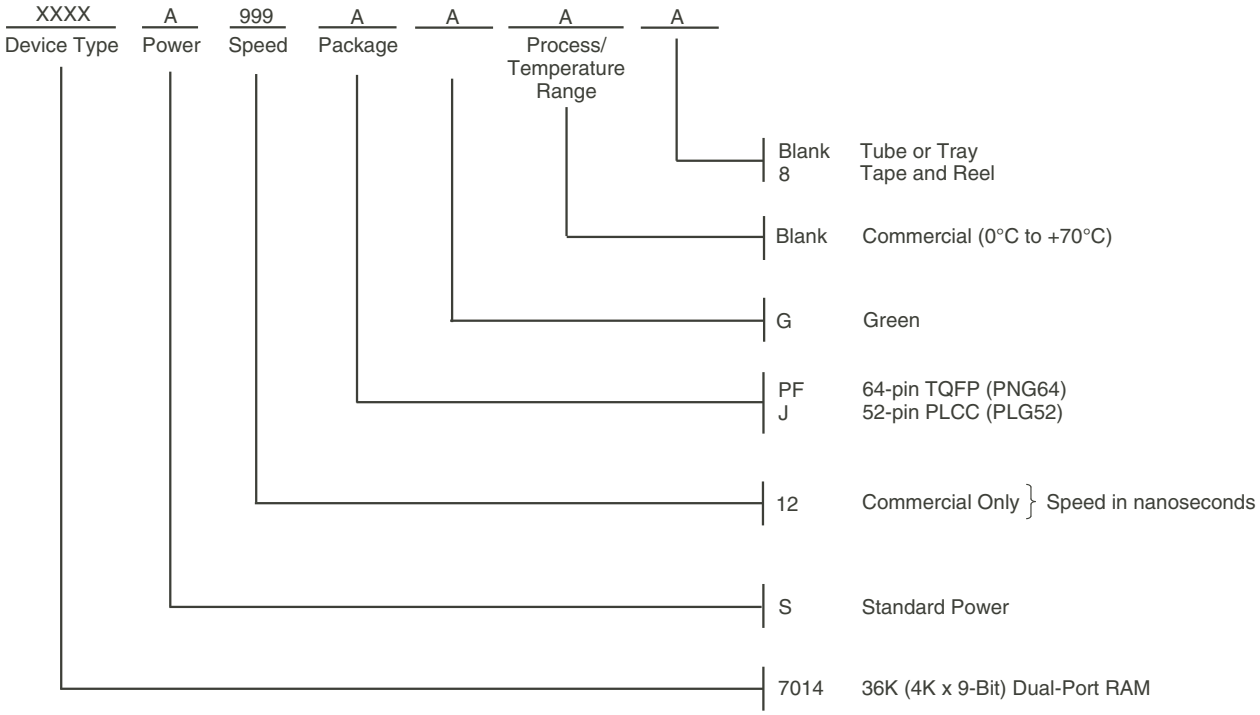
Truth Table I – Read/Write Control

Left or Right Port(1)			
R/$\overline{W}$	$\overline{OE}$	D0-8	**Function**
L	X	DATAIN	Data written into memory
H	L	DATAOUT	Data in memory output on port
X	H	Z	High-impedance outputs

2528 tbl 10

NOTE:
1. A_{OL} - A_{11L} is not equal to A_{OR} - A_{11R}.
'H' = HIGH,'L' = LOW, 'X' = Don't Care, and 'Z' = HIGH Impedance.

Ordering Information



NOTES:
LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02
Note that information regarding recently obsoleted parts is included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
12	7014S12JG	PLG52	PLCC	C
	7014S12JG8	PLG52	PLCC	C
	7014S12PFG	PNG64	TQFP	C
	7014S12PFG8	PNG64	TQFP	C

Datasheet Document History

01/06/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
	Page 2	Added additional notes to pin configurations
06/03/99:		Changed drawing format
	Page 1	Corrected DSC number

Datasheet Document History (con't)

03/10/00:		Added Industrial Temperature Ranges and deleted corresponding notes
		Replaced IDT logo
	Page 1	Made corrections to drawing
		Changed ±200mV to 0mV in notes
	Page 6	Made changes to drawings
05/19/00:	Page 3	Increased storage temperature parameter
		Clarified T_A parameter
10/16/01:	Page 2	Added date revision for pin configuration
	Pages 4, 5 & 7	Removed Industrial temp values and column headings for 15 & 25ns speeds from DC and AC Electrical Characteristics
	Page 9	Removed Industrial temp offering from 15 & 25ns ordering information
		Added Industrial temp footnote to ordering information
	Pages 1 & 9	Replaced TM logo with ® logo
04/04/06:	Page 1	Added green availability to features
	Page 9	Added green indicator to ordering information
12/11/08:	Page 9	Removed "IDT" from orderable part number
08/18/14:	Page 9	Added Tape and Reel to Ordering Information
	Page 2 & 9	The package codes PN84-1 & J52-1 changed to PN84 & J52 respectively to match standard package codes
03/16/16:	Page 2	Changed diagram for the PN64 pin configuration by rotating package pin labels and pin numbers 90 degrees counter clockwise to reflect pin 1 orientation and added pin 1 dot at pin 1
		Removed the PN64 chamfer and aligned the top and bottom pin labels in the standard direction
		Added the IDT logo to the PN64 pin configurations and changed the text to be in alignment with new diagram marking specs
		Removed the date revision indicator for each pin configuration
		Updated footnote references for PN64 pin configuration
	Page 4	Figure 3 Typical Output Derating Graph, corrected a typo
10/10/17:		Product Discontinuation Notice - PDN# SP-17-02
		Last time buy expires June 15, 2018
05/14/19:	Page 1	Removed Industrial speed grade offering and updated Commercial speed grade offering in Features
	Page 2	Changed diagram for the PLG52 pin configuration by rotating package pin labels and pin numbers 90 degrees clockwise to reflect pin 1 orientation and added pin 1 dot at pin 1
		Aligned the top and bottom pin labels in the standard direction
		Added the IDT logo to the PLG52 pin configuration and changed the text to be in alignment with new diagram marking specs
		Updated footnote references for PNG64 and PLG52
	Page 2 & 9	The package codes PN64 & J52 changed to PNG64 & PLG52 respectively to match standard package codes
	Page 9	Removed Industrial speed grade offering and updated Commercial speed grade offering in Ordering Information
		Removed industrial temp footnote from ordering information
		Revised LEAD FINISH note to indicate Obsolete
		Added Orderable Part Information
12/13/21:	Page 1 - 11	Source file updated to reflect previous Corporate Marketing rebranding
	Page 2	Package codes updated by removing IDT
	Page 10	Ordering information updated by removing green footnote reference

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