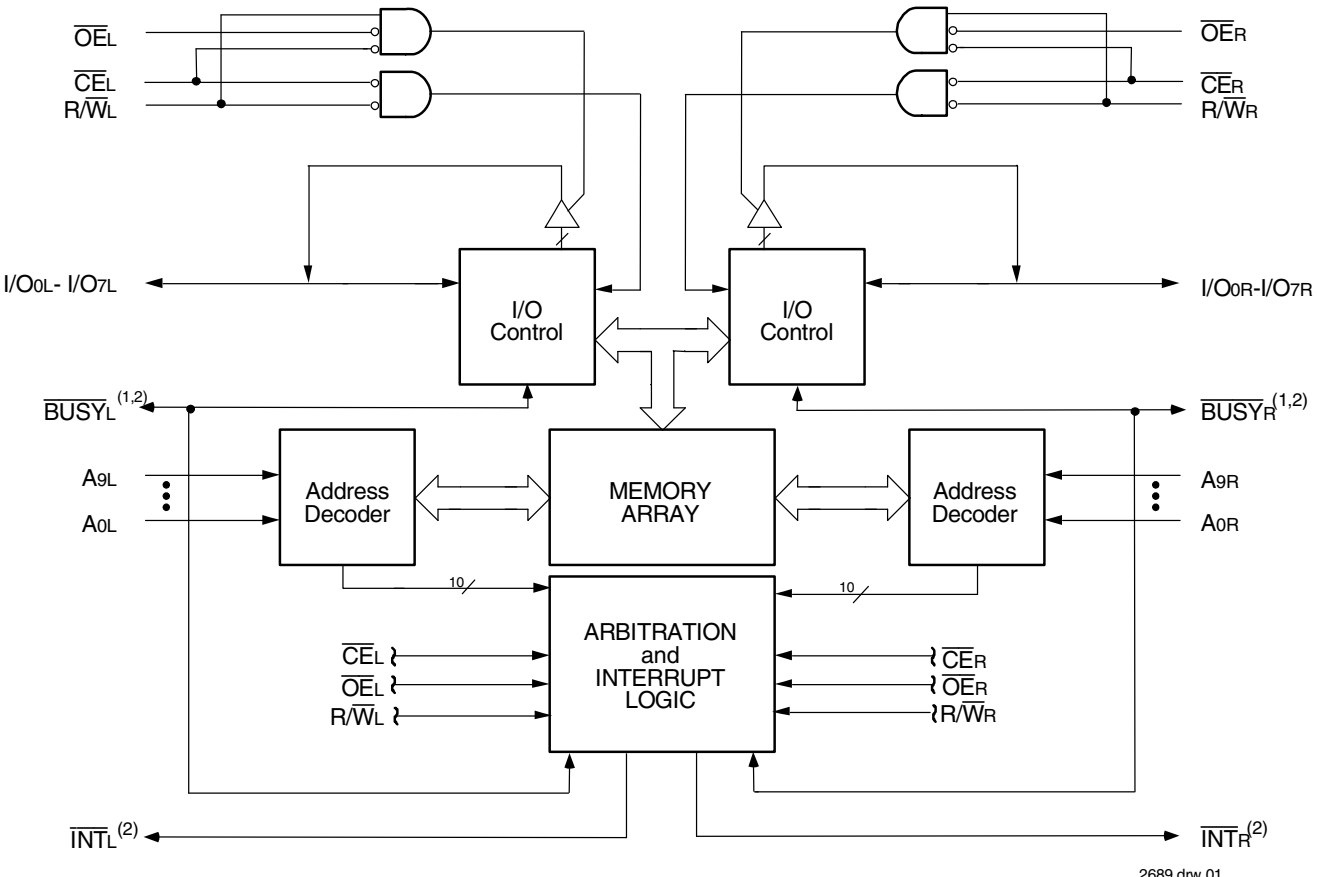
# HIGH SPEED 1K X 8 DUAL-PORT STATIC SRAM

**7130SA/LA**
**7140SA/LA**

## Features

- **High-speed access**
  - *Commercial: 20/25/35/55/100ns (max.)*
  - *Industrial: 25/55ns (max.)*
  - *Military: 25/35/55/100ns (max.)*
- **Low-power operation**
  - *IDT7130/IDT7140SA*
    *Active: 550mW (typ.)*
    *Standby: 5mW (typ.)*
  - *IDT7130/IDT7140LA*
    *Active: 550mW (typ.)*
    *Standby: 1mW (typ.)*
- **MASTER IDT7130 easily expands data bus width to 16-or-more-bits using SLAVE IDT7140**
- **On-chip port arbitration logic (IDT7130 Only)**
- **$\overline{BUSY}$ output flag on IDT7130; $\overline{BUSY}$ input on IDT7140**
- **$\overline{INT}$ flag for port-to-port communication**
- **Fully asynchronous operation from either port**
- **Battery backup operation–2V data retention (LA only)**
- **TTL-compatible, single 5V ±10% power supply**
- **Military product compliant to MIL-PRF-38535 QML**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Available in 48-pin DIP, LCC and Ceramic Flatpack, 52-pin PLCC, and 64-pin STQFP and TQFP**
- **Green parts available, see ordering information**

## Functional Block Diagram




2689 drw 01

**NOTES:**

1. IDT7130 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7140 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

## Description

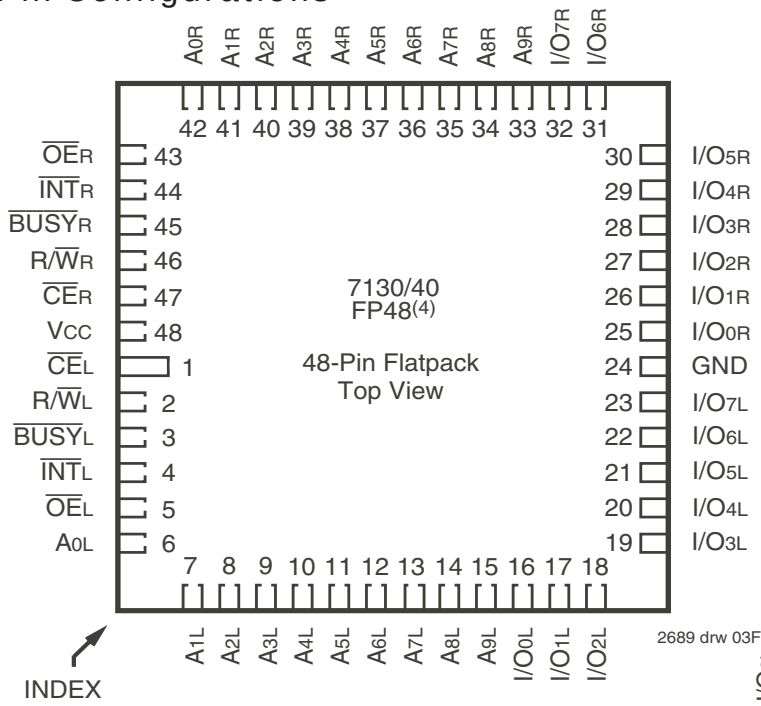
The IDT7130/IDT7140 are high-speed 1K x 8 Dual-Port Static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7140 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

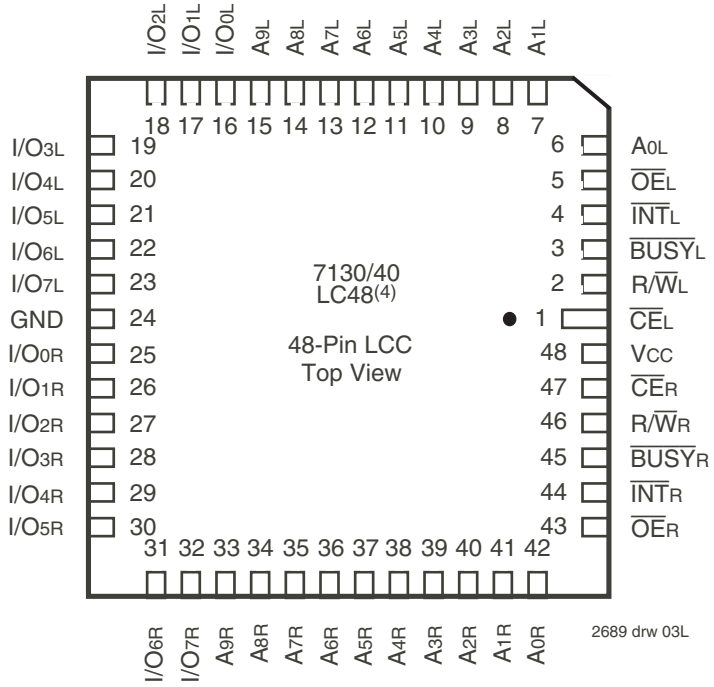
Fabricated using CMOS high-performance technology, these devices typically operate on only 550mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT7130/IDT7140 devices are packaged in 48-pin sidebraze or plastic DIPs, LCCs, flatpacks, 52-pin PLCC, and 64-pin TQFP and STQFP. Military grade products are manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## Pin Configurations[1,2,3]




2689 drw 03F

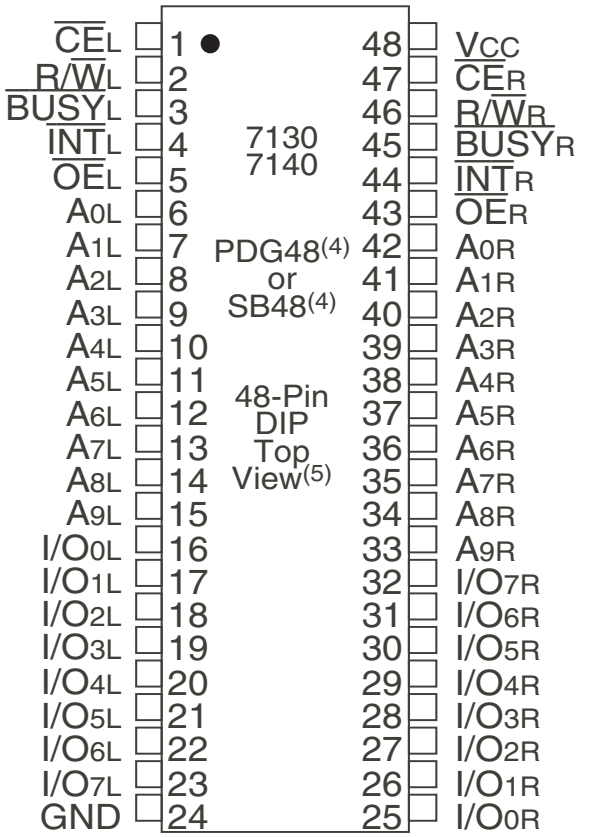



2689 drw 03L

**NOTES:**

1. All VCC pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. LC48 package body is approximately .57 in x .57 in x .68 in.
   FP48 package body is approximately .75 in x .75 in x .11 in.
4. This package code is used to reference the package diagram.

## Pin Configurations[1,2,3] (con't.)

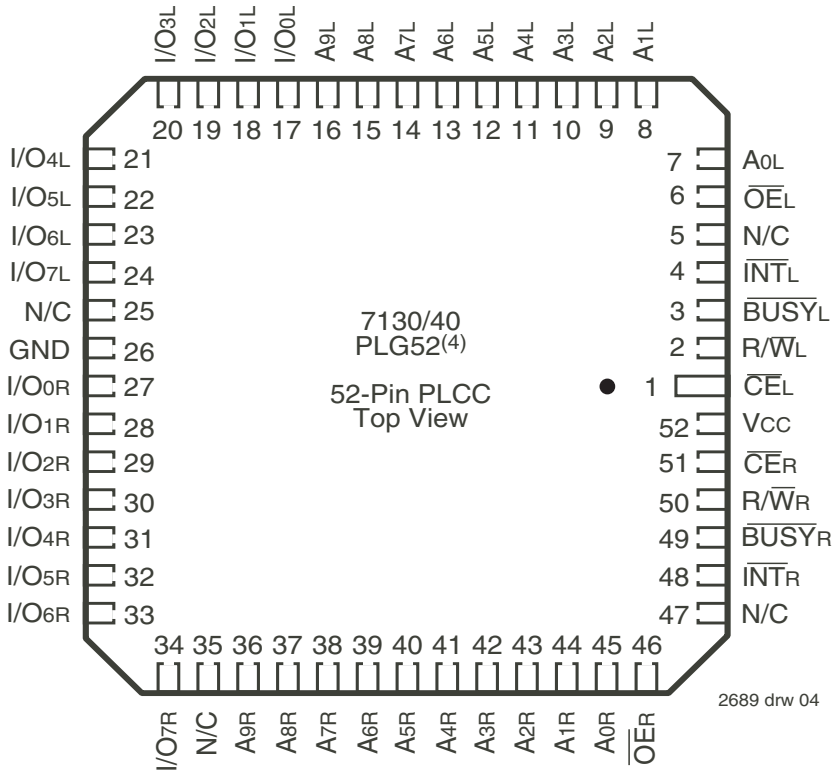



2689 drw 02

**NOTES:**

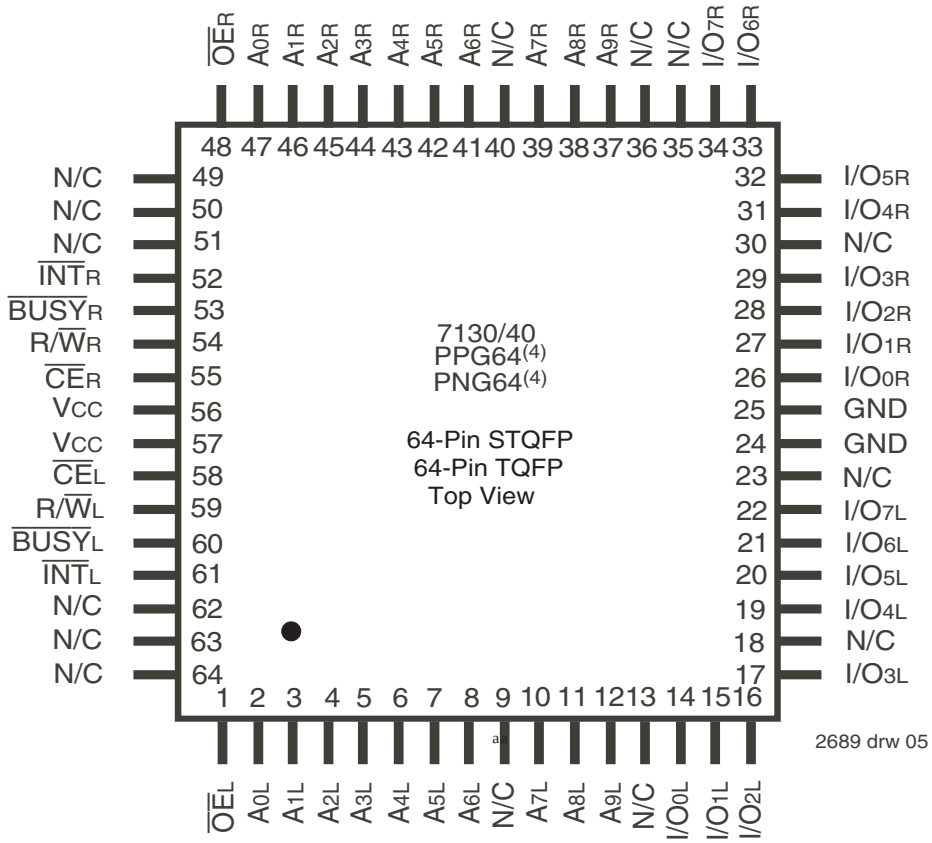
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. PDG48 package body is approximately .55 in x .61 in x .19 in. SB48 package body is approximately .62 in x 2.43 in x .15 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

## Pin Configurations[1,2,3] (con't.)




**NOTES:**
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. PLG52 package body is approximately .75 in x .75 in x .17 in.
4. This package code is used to reference the package diagram.

## Pin Configurations[1,2,3] (con't.)




**NOTES:**
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. PPG64 package body is approximately 10 mm x 10 mm x 1.4mm.
   PNG64 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram

## Absolute Maximum Ratings(1)

| Symbol | Rating | Commercial & Industrial | Military | Unit |
|---|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | -65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | -65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | 50 | 50 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{TERM}$ must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM}$ ≥ Vcc + 10%.

## Capacitance ($T_A$ = +25°C, f = 1.0MHz)

STQFP and TQFP Packages Only

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 9 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 3dV | 10 | pF |

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NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

## Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Vcc | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | — | 6.0(2) | V |
| $V_{IL}$ | Input Low Voltage | -0.5(1) | — | 0.8 | V |

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**NOTES:**
1. $V_{IL}$ (min.) ≥ -1.5V for pulse width less than 10ns.
2. $V_{TERM}$ must not exceed Vcc + 10%.

## Recommended Operating Temperature and Supply Voltage(1)

| Grade | Ambient Temperature | GND | Vcc |
|---|---|---|---|
| Military | -55°C to +125°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5.0V ± 10% |

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**NOTES:**
1. This is the parameter $T_A$. This is the "instant on" case temperature.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5.0V ± 10%)

| Symbol | Parameter | Test Conditions | 7130SA 7140SA | | 7130LA 7140LA | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $\|I_{LI}\|$ | Input Leakage Current(1) | Vcc = 5.5V, $V_{IN}$ = 0V to Vcc | — | 10 | — | 5 | µA |
| $\|I_{LO}\|$ | Output Leakage Current(1) | Vcc - 5.5V, $\overline{CE}$ = $V_{IH}$, $V_{OUT}$ = 0V to Vcc | — | 10 | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage ($I/O_0$-$I/O_7$) | $I_{OL}$ = 4mA | — | 0.4 | — | 0.4 | V |
| $V_{OL}$ | Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$) | $I_{OL}$ = 16mA | — | 0.5 | — | 0.5 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4mA | 2.4 | — | 2.4 | — | V |

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**NOTE:**
1. At Vcc ≤ 2.0V leakages are undefined.

# DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,5] ($V_{CC}$ = 5.0V ± 10%)

| Symbol | Parameter | Test Condition | Version | | 7130X20[2] 7140X20[2] Com'l Only Typ. | 7130X20[2] 7140X20[2] Com'l Only Max. | 7130X25 7140X25 Com'l, Ind & Military Typ. | 7130X25 7140X25 Com'l, Ind & Military Max. | 7130X35 7140X35 Com'l & Military Typ. | 7130X35 7140X35 Com'l & Military Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Dynamic Operating Current (Both Ports Active) | $\overline{CE}_L$ and $\overline{CE}_R$ = $V_{IL}$, Outputs Disabled f = $f_{MAX}$[3] | COM'L | SA | 110 | 250 | 110 | 220 | 110 | 165 | mA |
| | | | | LA | 110 | 200 | 110 | 170 | 110 | 120 | |
| | | | MIL & IND | SA | — | — | 110 | 280 | 110 | 230 | |
| | | | | LA | — | — | 110 | 220 | 110 | 170 | |
| $I_{SB1}$ | Standby Current (Both Ports - TTL Level Inputs) | $\overline{CE}_L$ and $\overline{CE}_R$ = $V_{IH}$ f = $f_{MAX}$[3] | COM'L | SA | 30 | 65 | 30 | 65 | 25 | 65 | mA |
| | | | | LA | 30 | 45 | 30 | 45 | 25 | 45 | |
| | | | MIL & IND | SA | — | — | 30 | 80 | 25 | 80 | |
| | | | | LA | — | — | 30 | 60 | 25 | 60 | |
| $I_{SB2}$ | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}_{"A"}$ = $V_{IL}$ and $\overline{CE}_{"B"}$ = $V_{IH}$[6] Active Port OutputsDisabled, f=$f_{MAX}$[3] | COM'L | SA | 65 | 165 | 65 | 150 | 50 | 125 | mA |
| | | | | LA | 65 | 125 | 65 | 115 | 50 | 90 | |
| | | | MIL & IND | SA | — | — | 65 | 160 | 50 | 150 | |
| | | | | LA | — | — | 65 | 125 | 50 | 115 | |
| $I_{SB3}$ | Full Standby Current (Both Ports - CMOS Level Inputs) | $\overline{CE}_L$ and $\overline{CE}_R$ ≥ $V_{CC}$ - 0.2V, $V_{IN}$ ≥ $V_{CC}$ - 0.2V or $V_{IN}$ ≤ 0.2V, f = 0[4] | COM'L | SA | 1.0 | 15 | 1.0 | 15 | 1.0 | 30 | mA |
| | | | | LA | 0.2 | 5 | 0.2 | 5 | 0.2 | 10 | |
| | | | MIL & IND | SA | — | — | 1.0 | 30 | — | — | |
| | | | | LA | — | — | 0.2 | 10 | — | — | |
| $I_{SB4}$ | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ $V_{CC}$ - 0.2V[6] $V_{IN}$ ≥ $V_{CC}$ - 0.2V or $V_{IN}$ ≤ 0.2V Active Port Outputs Disabled, f = $f_{MAX}$[3] | COM'L | SA | 60 | 155 | 60 | 145 | 45 | 110 | mA |
| | | | | LA | 60 | 115 | 60 | 105 | 45 | 85 | |
| | | | MIL & IND | SA | — | — | 60 | 155 | 45 | 145 | |
| | | | | LA | — | — | 60 | 115 | 45 | 105 | |

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| Symbol | Parameter | Test Condition | Version | | 7130X55 7140X55 Com'l, Ind & Military Typ. | 7130X55 7140X55 Com'l, Ind & Military Max. | 7130X100 7140X100 Com'l, Ind & Military Typ. | 7130X100 7140X100 Com'l, Ind & Military Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Dynamic Operating Current (Both Ports Active) | $\overline{CE}_L$ and $\overline{CE}_R$ = $V_{IL}$, Outputs Disabled f = $f_{MAX}$[3] | COM'L | SA | 110 | 155 | 110 | 155 | mA |
| | | | | LA | 110 | 110 | 110 | 110 | |
| | | | MIL & IND | SA | 110 | 190 | 110 | 190 | |
| | | | | LA | 110 | 140 | 110 | 140 | |
| $I_{SB1}$ | Standby Current (Both Ports - TTL Level Inputs) | $\overline{CE}_L$ and $\overline{CE}_R$ = $V_{IH}$ f = $f_{MAX}$[3] | COM'L | SA | 20 | 65 | 20 | 55 | mA |
| | | | | LA | 20 | 35 | 20 | 35 | |
| | | | MIL & IND | SA | 20 | 65 | 20 | 65 | |
| | | | | LA | 20 | 45 | 20 | 45 | |
| $I_{SB2}$ | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}_{"A"}$ = $V_{IL}$ and $\overline{CE}_{"B"}$ = $V_{IH}$[6] Active Port Outputs Disabled, f=$f_{MAX}$[3] | COM'L | SA | 40 | 110 | 40 | 110 | mA |
| | | | | LA | 40 | 75 | 40 | 75 | |
| | | | MIL & IND | SA | 40 | 125 | 40 | 125 | |
| | | | | LA | 40 | 90 | 40 | 90 | |
| $I_{SB3}$ | Full Standby Current (Both Ports - CMOS Level Inputs) | $\overline{CE}_L$ and $\overline{CE}_R$ ≥ $V_{CC}$ - 0.2V, $V_{IN}$ ≥ $V_{CC}$ - 0.2V or $V_{IN}$ ≤ 0.2V, f = 0[4] | COM'L | SA | 1.0 | 15 | 1.0 | 15 | mA |
| | | | | LA | 0.2 | 4 | 0.2 | 4 | |
| | | | MIL & IND | SA | 1.0 | 30 | 1.0 | 30 | |
| | | | | LA | 0.2 | 10 | 0.2 | 10 | |
| $I_{SB4}$ | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ $V_{CC}$ - 0.2V[6] $V_{IN}$ ≥ $V_{CC}$ - 0.2V or $V_{IN}$ ≤ 0.2V Active Port Outputs Disabled, f = $f_{MAX}$[3] | COM'L | SA | 40 | 100 | 40 | 95 | mA |
| | | | | LA | 40 | 70 | 40 | 70 | |
| | | | MIL & IND | SA | 40 | 110 | 40 | 110 | |
| | | | | LA | 40 | 85 | 40 | 80 | |

2689 tbl 06b

**NOTES:**

1. 'X' in part numbers indicates power rating (SA or LA).
2. PLCC , TQFP and STQFP packages only.
3. At f = $f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/$t_{CYC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
4. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
5. Vcc = 5V, $T_A$=+25°C for Typ and is not production tested. Vcc DC = 100 mA (Typ)
6. Port "A" may be either left or right port. Port "B" is opposite from port "A".

## Data Retention Characteristics (LA Version Only)

| Symbol | Parameter | Test Condition | | 7130LA/7140LA Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | | 2.0 | — | — | V |
| $I_{CCDR}$ | Data Retention Current | $V_{CC}$ = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V | MIL. & IND. | — | 100 | 4000 | µA |
| | | | COM'L. | — | 100 | 1500 | |
| $t_{CDR}$[3] | Chip Deselect to Data Retention Time | $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V | | 0 | — | — | ns |
| $t_R$[3] | Operation Recovery Time | | | $t_{RC}$[2] | — | — | ns |

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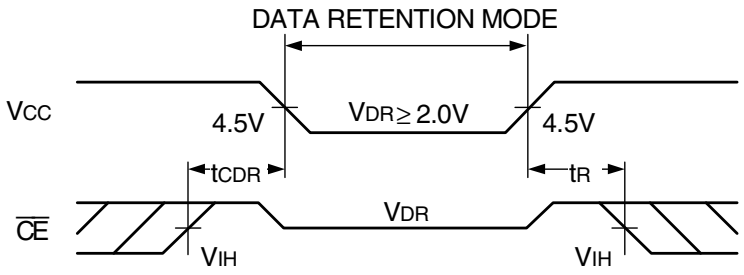
**NOTES:**
1. $V_{CC}$ = 2V, $T_A$ = +25°C, and is not production tested.
2. $t_{RC}$ = Read Cycle Time
3. This parameter is guaranteed but not production tested.

## Data Retention Waveform




2692 drw 06

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | Figures 1,2 and 3 |

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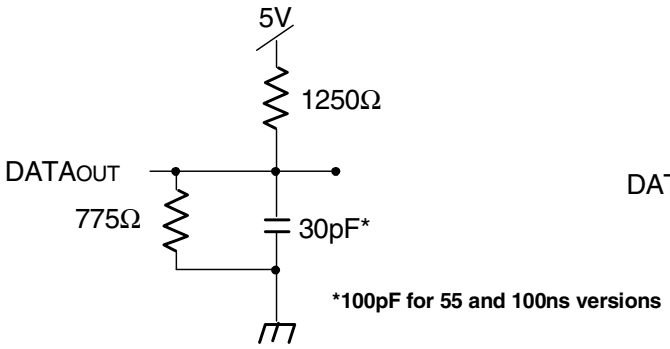



**Figure 1. Output Test Load**

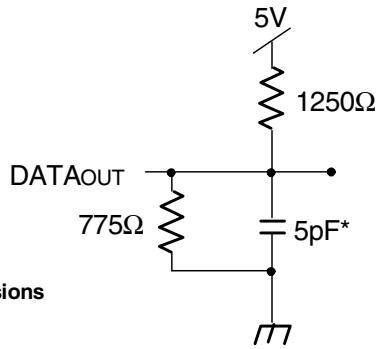
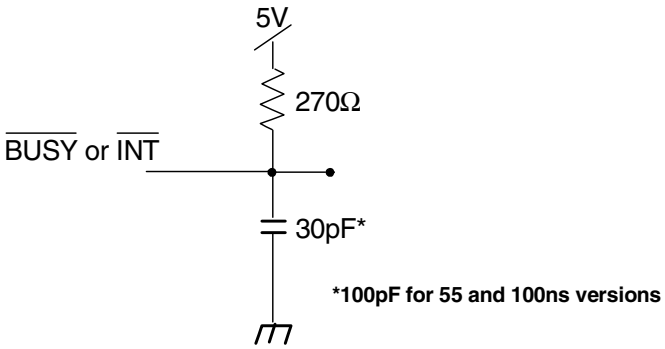



**Figure 2. Output Test Load**
**(for $t_{HZ}$, $t_{LZ}$, $t_{WZ}$, and $t_{OW}$)**
* including scope and jig




2689 drw 07

**Figure 3. $\overline{BUSY}$ and $\overline{INT}$**
**AC Output Test Load**

## AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range[3]

| Symbol | Parameter | 7130X20[2] 7140X20[2] Com'l Only | | 7130X25 7140X25 Com'l, Ind & Military | | 7130X35 7140X35 Com'l & Military | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 20 | — | 25 | — | 35 | — | ns |
| $t_{AA}$ | Address Access Time | — | 20 | — | 25 | — | 35 | ns |
| $t_{ACE}$ | Chip Enable Access Time | — | 20 | — | 25 | — | 35 | ns |
| $t_{AOE}$ | Output Enable Access Time | — | 11 | — | 12 | — | 20 | ns |
| $t_{OH}$ | Output Hold from Address Change | 3 | — | 3 | — | 3 | — | ns |
| $t_{LZ}$ | Output Low-Z Time[1,4] | 0 | — | 0 | — | 0 | — | ns |
| $t_{HZ}$ | Output High-Z Time[1,4] | — | 10 | — | 10 | — | 15 | ns |
| $t_{PU}$ | Chip Enable to Power Up Time[4] | 0 | — | 0 | — | 0 | — | ns |
| $t_{PD}$ | Chip Disable to Power Down Time[4] | — | 20 | — | 25 | — | 35 | ns |

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| Symbol | Parameter | 7130X55 7140X55 Com'l, Ind & Military | | 7130X100 7140X100 Com'l, Ind & Military | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 55 | — | 100 | — | ns |
| $t_{AA}$ | Address Access Time | — | 55 | — | 100 | ns |
| $t_{ACE}$ | Chip Enable Access Time | — | 55 | — | 100 | ns |
| $t_{AOE}$ | Output Enable Access Time | — | 25 | — | 40 | ns |
| $t_{OH}$ | Output Hold from Address Change | 3 | — | 10 | — | ns |
| $t_{LZ}$ | Output Low-Z Time[1,4] | 5 | — | 5 | — | ns |
| $t_{HZ}$ | Output High-Z Time[1,4] | — | 25 | — | 40 | ns |
| $t_{PU}$ | Chip Enable to Power Up Time[4] | 0 | — | 0 | — | ns |
| $t_{PD}$ | Chip Disable to Power Down Time[4] | — | 50 | — | 50 | ns |

2689 tbl 09b

**NOTES:**
1. Transition is measured 0mV from Low or High-impedance voltage Output Test Load (Figure 2).
2. PLCC, TQFP and STQFP packages only.
3. 'X' in part numbers indicates power rating (SA or LA).
4. This parameter is guaranteed by device characterization, but is not production tested.

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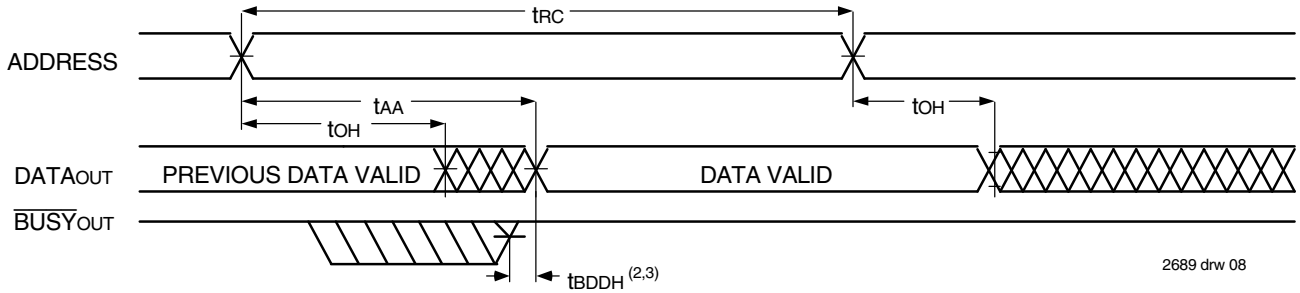
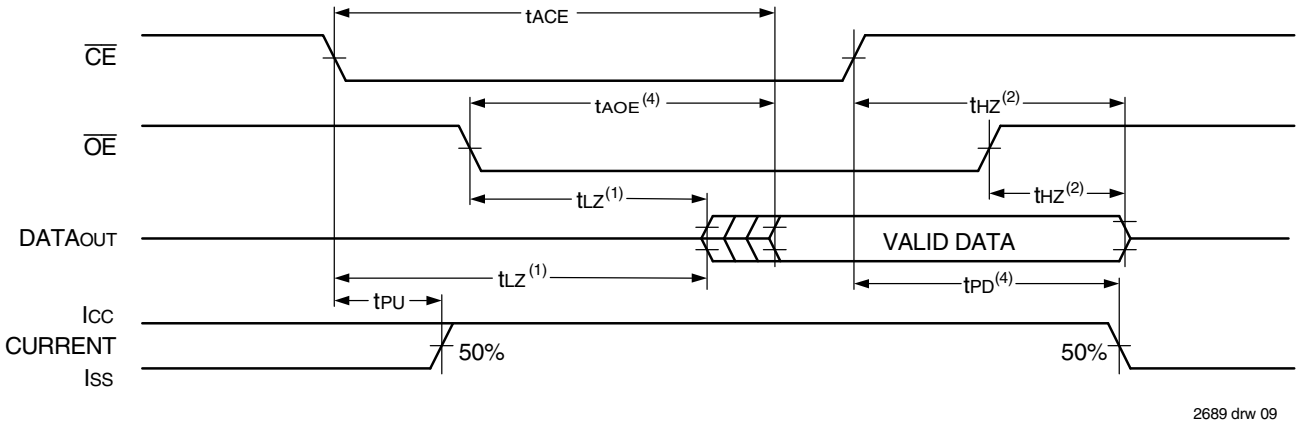
## Timing Waveform of Read Cycle No. 1, Either Side(1)




**NOTES:**
1. R/$\overline{W}$ = $V_{IH}$, $\overline{CE}$ = $V_{IL}$, and is $\overline{OE}$ = $V_{IL}$. Address is valid prior to the coincidental with $\overline{CE}$ transition LOW.
2. $t_{BDD}$ delay is required only in the case where the opposite port is completing a write operation to the same the address location. For simultaneous read operations, $\overline{BUSY}$ has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last $t_{AOE}$, $t_{ACE}$, $t_{AA}$, and $t_{BDD}$.

## Timing Waveform of Read Cycle No. 2, Either Side(3)




**NOTES:**
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = $V_{IH}$ and $\overline{OE}$ = $V_{IL}$, and the address is valid prior to or coincidental with $\overline{CE}$ transition LOW.
4. Start of valid data depends on which timing becomes effective last $t_{AOE}$, $t_{ACE}$, $t_{AA}$, and $t_{BDD}$.

## AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range[5]

| Symbol | Parameter | 7130X20[2] 7140X20[2] Com'l Only | | 7130X25 7140X25 Com'l, Ind & Military | | 7130X35 7140X35 Com'l & Military | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **WRITE CYCLE** | | | | | | | | |
| $t_{WC}$ | Write Cycle Time[3] | 20 | — | 25 | — | 35 | — | ns |
| $t_{EW}$ | Chip Enable to End-of-Write | 15 | — | 20 | — | 30 | — | ns |
| $t_{AW}$ | Address Valid to End-of-Write | 15 | — | 20 | — | 30 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width[4] | 15 | — | 15 | — | 25 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{DW}$ | Data Valid to End-of-Write | 10 | — | 12 | — | 15 | — | ns |
| $t_{HZ}$ | Output High-Z Time[1] | — | 10 | — | 10 | — | 15 | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{WZ}$ | Write Enable to Output in High-Z[1] | — | 10 | — | 10 | — | 15 | ns |
| $t_{OW}$ | Output Active from End-of-Write[1] | 0 | — | 0 | — | 0 | — | ns |

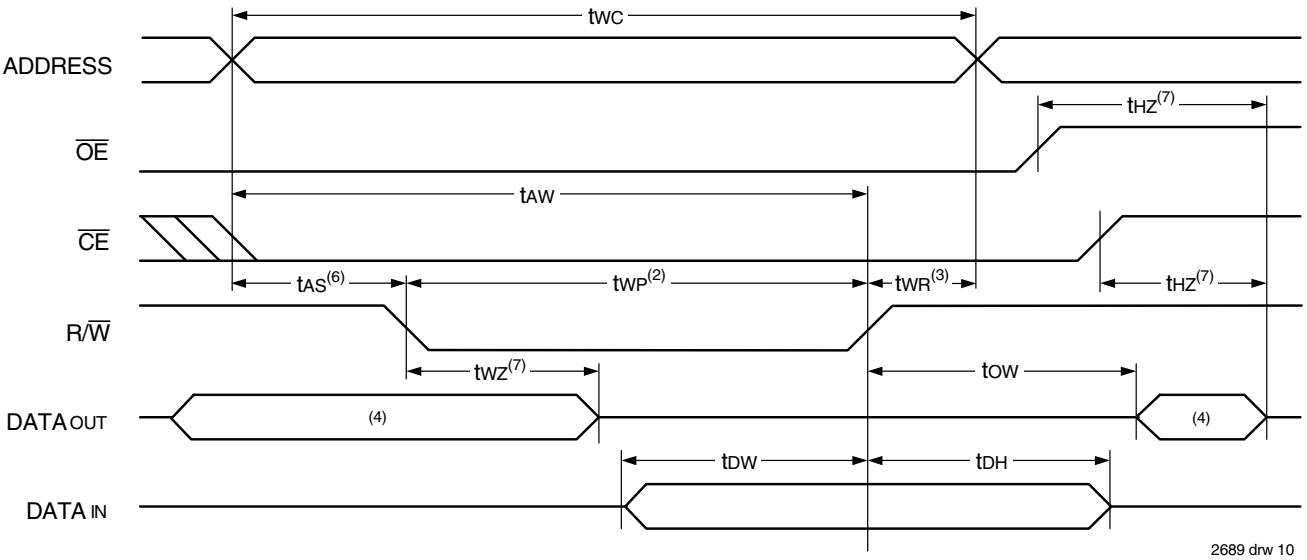
2689 tbl 10a

| Symbol | Parameter | 7130X55 7140X55 Com'l, Ind & Military | | 7130X100 7140X100 Com'l, Ind & Military | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **WRITE CYCLE** | | | | | | |
| $t_{WC}$ | Write Cycle Time[3] | 55 | — | 100 | — | ns |
| $t_{EW}$ | Chip Enable to End-of-Write | 40 | — | 90 | — | ns |
| $t_{AW}$ | Address Valid to End-of-Write | 40 | — | 90 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width[4] | 30 | — | 55 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | ns |
| $t_{DW}$ | Data Valid to End-of-Write | 20 | — | 40 | — | ns |
| $t_{HZ}$ | Output High-Z Time[1] | — | 25 | — | 40 | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | 0 | — | ns |
| $t_{WZ}$ | Write Enable to Output in High-Z[1] | — | 25 | — | 40 | ns |
| $t_{OW}$ | Output Active from End-of-Write[1] | 0 | — | 0 | — | ns |

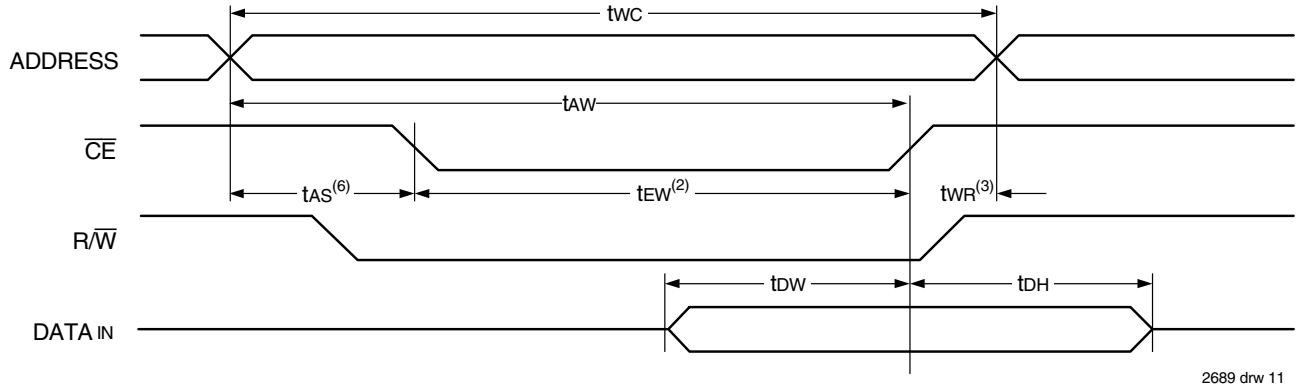
2689 tbl 10b

**NOTES:**
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2). This parameter is guaranteed by device characterization but is not production tested.
2. PLCC, TQFP and STQFP packages only.
3. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$, since $R/\overline{W} = V_{IL}$ must occur after $t_{BAA}$.
4. If $\overline{OE}$ is LOW during a $R/\overline{W}$ controlled write cycle, the write pulse width must be the larger of $t_{WP}$ or ($t_{WZ} + t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is HIGH during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified $t_{WP}$.
5. 'X' in part numbers indicates power rating (SA or LA).

## Timing Waveform of Write Cycle No. 1, (R/$\overline{W}$ Controlled Timing)(1,5,8)




## Timing Waveform of Write Cycle No. 2, ($\overline{CE}$ Controlled Timing)(1,5)




**NOTES:**

1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap ($t_{EW}$ or $t_{WP}$) of $\overline{CE}$ = $V_{IL}$ and R/$\overline{W}$ = $V_{IL}$.
3. $t_{WR}$ is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the HIGH impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of $t_{WP}$ or ($t_{WZ}$ + $t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified $t_{WP}$.

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(7)

| Symbol | Parameter | 7130X20(1) 7140X20(1) Com'l Only | | 7130X25 7140X25 Com'l, Ind & Military | | 7130X35 7140X35 Com'l & Military | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **$\overline{BUSY}$ TIMING (For MASTER IDT 7130)** | | | | | | | | |
| $t_{BAA}$ | $\overline{BUSY}$ Access Time from Address | — | 20 | — | 20 | — | 20 | ns |
| $t_{BDA}$ | $\overline{BUSY}$ Disable Time from Address | — | 20 | — | 20 | — | 20 | ns |
| $t_{BAC}$ | $\overline{BUSY}$ Access Time from Chip Enable | — | 20 | — | 20 | — | 20 | ns |
| $t_{BDC}$ | $\overline{BUSY}$ Disable Time from Chip Enable | — | 20 | — | 20 | — | 20 | ns |
| $t_{WH}$ | Write Hold After $\overline{BUSY}$(6) | 12 | — | 15 | — | 20 | — | ns |
| $t_{WDD}$ | Write Pulse to Data Delay(2) | — | 40 | — | 50 | — | 60 | ns |
| $t_{DDD}$ | Write Data Valid to Read Data Delay(2) | — | 30 | — | 35 | — | 35 | ns |
| $t_{APS}$ | Arbitration Priority Set-up Time(3) | 5 | — | 5 | — | 5 | — | ns |
| $t_{BDD}$ | $\overline{BUSY}$ Disable to Valid Data(4) | — | 25 | — | 35 | — | 35 | ns |
| **$\overline{BUSY}$ INPUT TIMING (For SLAVE IDT 7140)** | | | | | | | | |
| $t_{WB}$ | Write to $\overline{BUSY}$ Input(5) | 0 | — | 0 | — | 0 | — | ns |
| $t_{WH}$ | Write Hold After $\overline{BUSY}$(6) | 12 | — | 15 | — | 20 | — | ns |
| $t_{WDD}$ | Write Pulse to Data Delay(2) | — | 40 | — | 50 | — | 60 | ns |
| $t_{DDD}$ | Write Data Valid to Read Data Delay(2) | — | 30 | — | 35 | — | 35 | ns |

2689 tbl 11a

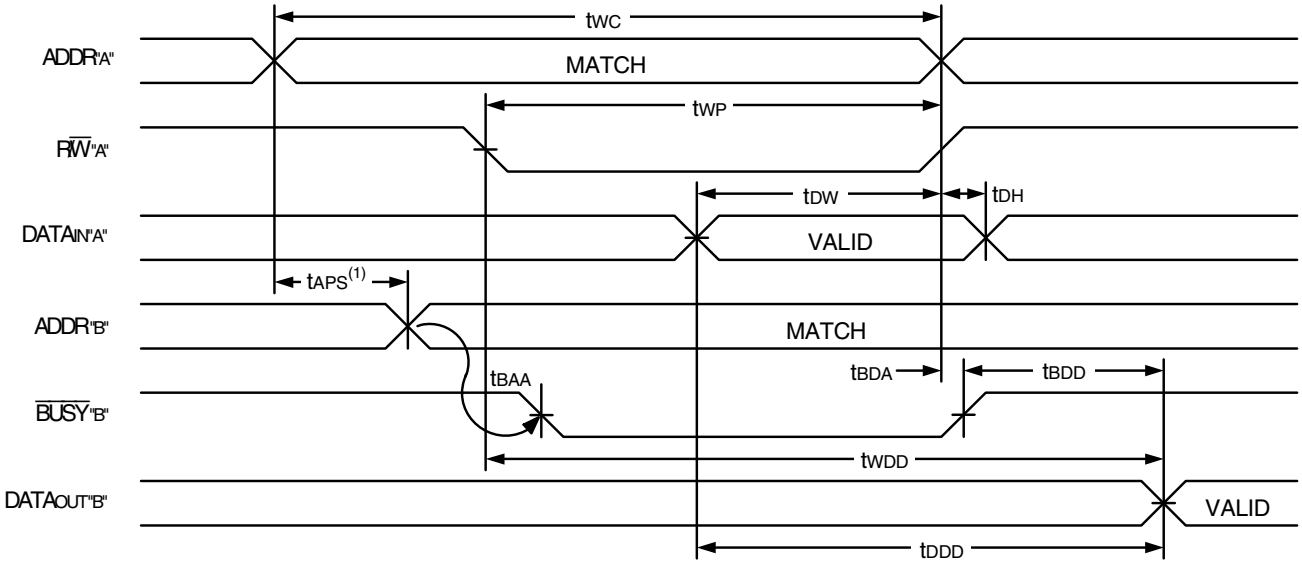
| Symbol | Parameter | 7130X55 7140X55 Com'l, Ind & Military | | 7130X100 7140X100 Com'l, Ind & Military | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **$\overline{BUSY}$ TIMING (For MASTER IDT 7130)** | | | | | | |
| $t_{BAA}$ | $\overline{BUSY}$ Access Time from Address] | — | 30 | — | 50 | ns |
| $t_{BDA}$ | $\overline{BUSY}$ Disable Time from Address | — | 30 | — | 50 | ns |
| $t_{BAC}$ | $\overline{BUSY}$ Access Time from Chip Enable | — | 30 | — | 50 | ns |
| $t_{BDC}$ | $\overline{BUSY}$ Disable Time from Chip Enable | — | 30 | — | 50 | ns |
| $t_{WH}$ | Write Hold After $\overline{BUSY}$(6) | 20 | — | 20 | — | ns |
| $t_{WDD}$ | Write Pulse to Data Delay(2) | — | 80 | — | 120 | ns |
| $t_{DDD}$ | Write Data Valid to Read Data Delay(2) | — | 55 | — | 100 | ns |
| $t_{APS}$ | Arbitration Priority Set-up Time(3) | 5 | — | 5 | — | ns |
| $t_{BDD}$ | $\overline{BUSY}$ Disable to Valid Data(4) | — | 55 | — | 65 | ns |
| **$\overline{BUSY}$ INPUT TIMING (For SLAVE IDT 7140)** | | | | | | |
| $t_{WB}$ | Write to $\overline{BUSY}$ Input(5) | 0 | — | 0 | — | ns |
| $t_{WH}$ | Write Hold After $\overline{BUSY}$(6) | 20 | — | 20 | — | ns |
| $t_{WDD}$ | Write Pulse to Data Delay(2) | — | 80 | — | 120 | ns |
| $t_{DDD}$ | Write Data Valid to Read Data Delay(2) | — | 55 | — | 100 | ns |

2689 tbl 11b

**NOTES:**

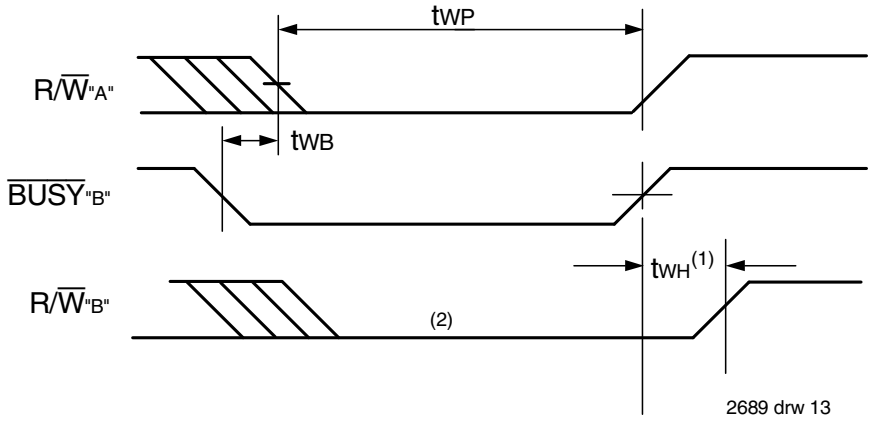
1. PLCC, TQFP and STQFP packages only.
2. Port-to-port delay through RAM cells from the writing port to the reading port, refer to "Timing Waveform of Write with Port -to-Port Read and $\overline{BUSY}$."
3. To ensure that the earlier of the two ports wins.
4. $t_{BDD}$ is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
5. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'.
6. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.
7. 'X' in part numbers indicates power rating (S or L).

## Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (2,3,4)



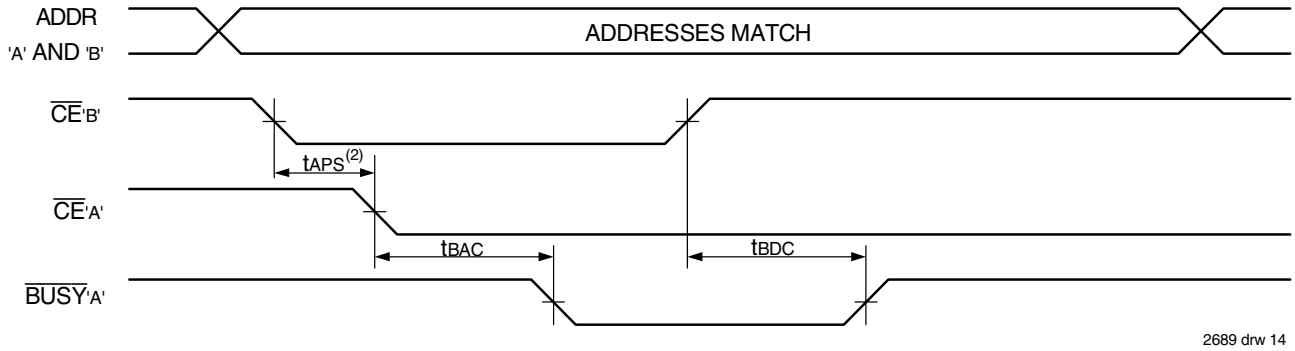

**NOTES:**
1. To ensure that the earlier of the two ports wins. $t_{BDD}$ is ignored for slave (IDT7140).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".

## Timing Waveform of Write with $\overline{BUSY}$ (3)



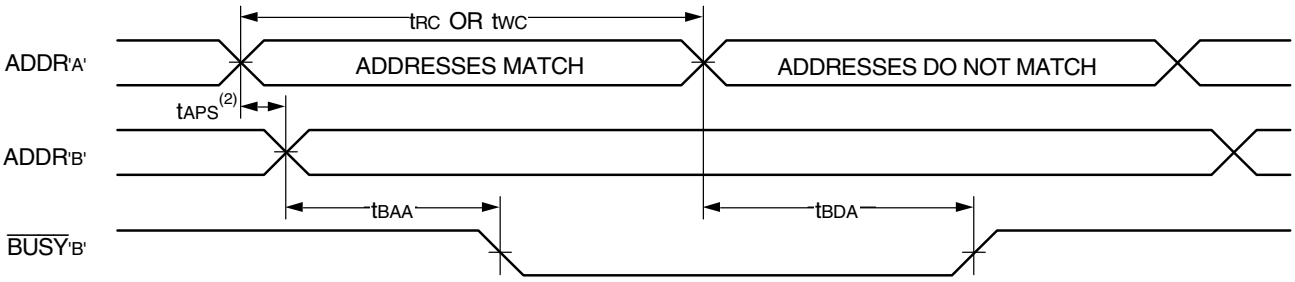

**NOTES:**
1. $t_{WH}$ must be met for both BUSY Input (IDT7140, slave) or Output (IDT7130 master).
2. $\overline{BUSY}$ is asserted on port "B" blocking $R/\overline{W}$"B", until $\overline{BUSY}$"B" goes HIGH.
3. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is opposite from port "A".

## Timing Waveform of $\overline{\text{BUSY}}$ Arbitration Controlled by $\overline{\text{CE}}$ Timing(1)




2689 drw 14

## Timing Waveform by $\overline{\text{BUSY}}$ Arbitration Controlled by Address Match Timing(1)




2689 drw 15

**NOTES:**
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If $t_{APS}$ is not satisfied, the $\overline{\text{BUSY}}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{\text{BUSY}}$ will be asserted (7130 only).

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(2)

| | | 7130X20(1) 7140X20(1) Com'l Only | | 7130X25 7140X25 Com'l, Ind & Military | | 7130X35 7140X35 Com'l & Military | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Unit** |
| **INTERRUPT TIMING** | | | | | | | | |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{INS}$ | Interrupt Set Time | — | 20 | — | 25 | — | 25 | ns |
| $t_{INR}$ | Interrupt Reset Time | — | 20 | — | 25 | — | 25 | ns |

2689 tbl 12a

**NOTES:**
1. PLCC, TQFP and STQFP package only.
2. 'X' in part numbers indicates power rating (SA or LA).

## AC Electrical characteristics Over the Operating Temperature and Supply Voltage Range(1)

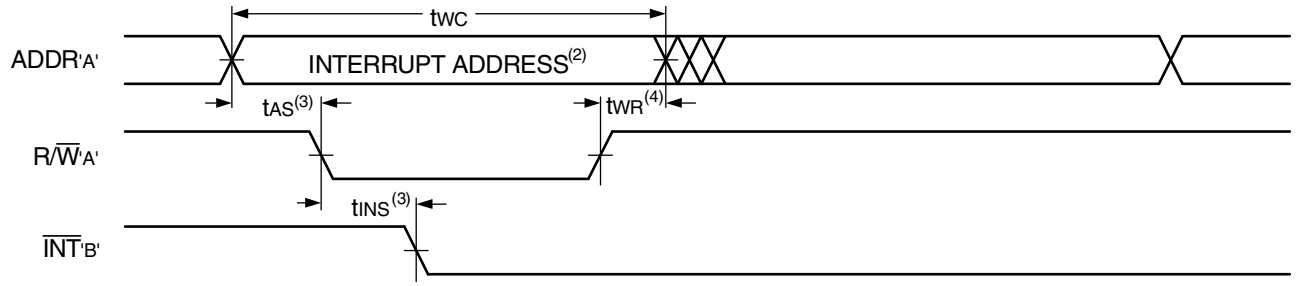
| | | 7130X55 7140X55 Com'l, Ind & Military | | 7130X100 7140X100 Com'l, Ind & Military | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Unit** |
| **INTERRUPT TIMING** | | | | | | |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | ns |
| $t_{INS}$ | Interrupt Set Time | — | 45 | — | 60 | ns |
| $t_{INR}$ | Interrupt Reset Time | — | 45 | — | 60 | ns |

2689 tbl 12b

**NOTES:**
1. 'X' in part numbers indicates power rating (SA or LA).

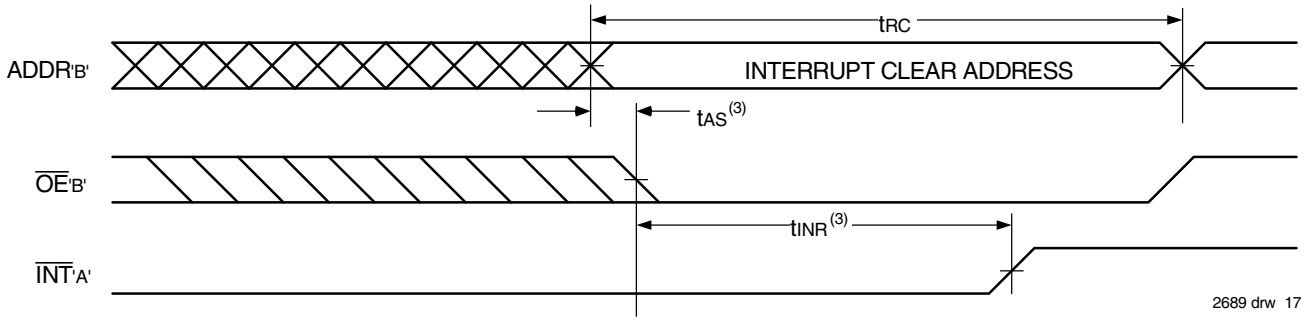
## Timing Waveform of Interrupt Mode(1)

### $\overline{INT}$ Set:




2689 drw 16

### $\overline{INT}$ Clear:




2689 drw 17

**NOTES:**.
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interrupt Truth Table II.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

# Truth Tables

## Truth Table I — Non-Contention Read/Write Control(4)

| Inputs(1) | | | | Function |
|---|---|---|---|---|
| R/$\overline{W}$ | $\overline{CE}$ | $\overline{OE}$ | $D_{0-7}$ | |
| X | H | X | Z | Port Disabled and in Power-Down Mode, $I_{SB2}$ or $I_{SB4}$ |
| X | H | X | Z | $\overline{CE}_R$ = $\overline{CE}_L$ = $V_{IH}$, Power-Down Mode, $I_{SB1}$ or $I_{SB3}$ |
| L | L | X | $DATA_{IN}$ | Data on Port Written into Memory(2) |
| H | L | L | $DATA_{OUT}$ | Data in Memory Output on Port(3) |
| H | L | H | Z | High Impedance Outputs |

2689 tbl 13

**NOTES:**
1. $A_{0L}$ – $A_{10L}$ ≠ $A_{0R}$ – $A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see $t_{WDD}$ and $t_{DDD}$ timing.
4. 'H' = $V_{IH}$, 'L' = $V_{IL}$, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

## Truth Table II — Interrupt Flag(1,4)

| Left Port | | | | | Right Port | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| R/$\overline{W}_L$ | $\overline{CE}_L$ | $\overline{OE}_L$ | $A_{9L}$-$A_{0L}$ | $\overline{INT}_L$ | R/$\overline{W}_R$ | $\overline{CE}_R$ | $\overline{OE}_R$ | $A_{9R}$-$A_{0R}$ | $\overline{INT}_R$ | Function |
| L | L | X | 3FF | X | X | X | X | X | L(2) | Set Right $\overline{INT}_R$ Flag |
| X | X | X | X | X | X | L | L | 3FF | H(3) | Reset Right $\overline{INT}_R$ Flag |
| X | X | X | X | L(3) | L | L | X | 3FE | X | Set Left $\overline{INT}_L$ Flag |
| X | L | L | 3FE | H(2) | X | X | X | X | X | Reset Left $\overline{INT}_L$ Flag |

2689 tbl 14

**NOTES**:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = $V_{IH}$
2. If $\overline{BUSY}_L$ = $V_{IL}$, then No Change.
3. If $\overline{BUSY}_R$ = $V_{IL}$, then No Change.
4. 'H' = HIGH,' L' = LOW,' X' = DON'T CARE

## Truth Table III — Address $\overline{BUSY}$ Arbitration

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| $\overline{CE}_L$ | $\overline{CE}_R$ | $A_{0L}$-$A_{9L}$<br>$A_{0R}$-$A_{9R}$ | $\overline{BUSY}_L$(1) | $\overline{BUSY}_R$(1) | Function |
| X | X | NO MATCH | H | H | Normal |
| H | X | MATCH | H | H | Normal |
| X | H | MATCH | H | H | Normal |
| L | L | MATCH | (2) | (2) | Write Inhibit(3) |

2689 tbl 15

**NOTES:**
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs for IDT7130 (master). Both are inputs for IDT7140 (slave). $\overline{BUSY}_X$ outputs on the IDT7130 are open drain, not push-pull outputs. On slaves the $\overline{BUSY}_X$ input internally inhibits writes.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If $t_{APS}$ is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

## Functional Description

The IDT7130/IDT7140 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7130/IDT7140 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = $V_{IH}$). When a port is enabled, access to the entire memory array is permitted.

## Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 3FE (HEX), where a write is defined as the $\overline{CE}_R$ = R/$\overline{W}_R$ = $V_{IL}$ per Truth Table II. The left port clears the interrupt by accessing address location 3FE when $\overline{CE}_L$ = $\overline{OE}_L$ = $V_{IL}$, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location 3FF. The message (8 bits) at 3FE or 3FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FE and 3FF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table II for the interrupt operation.

## Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is “Busy”. The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{BUSY}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation. In slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the $\overline{BUSY}$ pin for that port LOW.

The $\overline{BUSY}$ outputs on the IDT7130 RAM (Master) are open drain type outputs and require open drain resistors to operate. If these RAMs are being expanded in depth, then the $\overline{BUSY}$ indication for the resulting array does not require the use of an external AND gate.

## Width Expansion with Busy Logic Master/Slave Arrays

When expanding an RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7130/IDT7140 RAMs the $\overline{BUSY}$ pin is an output if the part is Master (IDT7130), and the $\overline{BUSY}$ pin is an input if the part is a Slave (IDT7140) as shown in Figure 3.

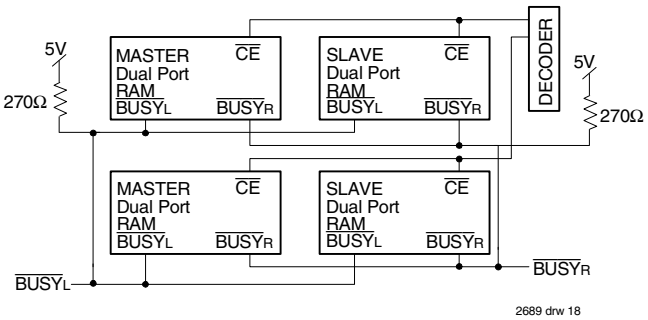
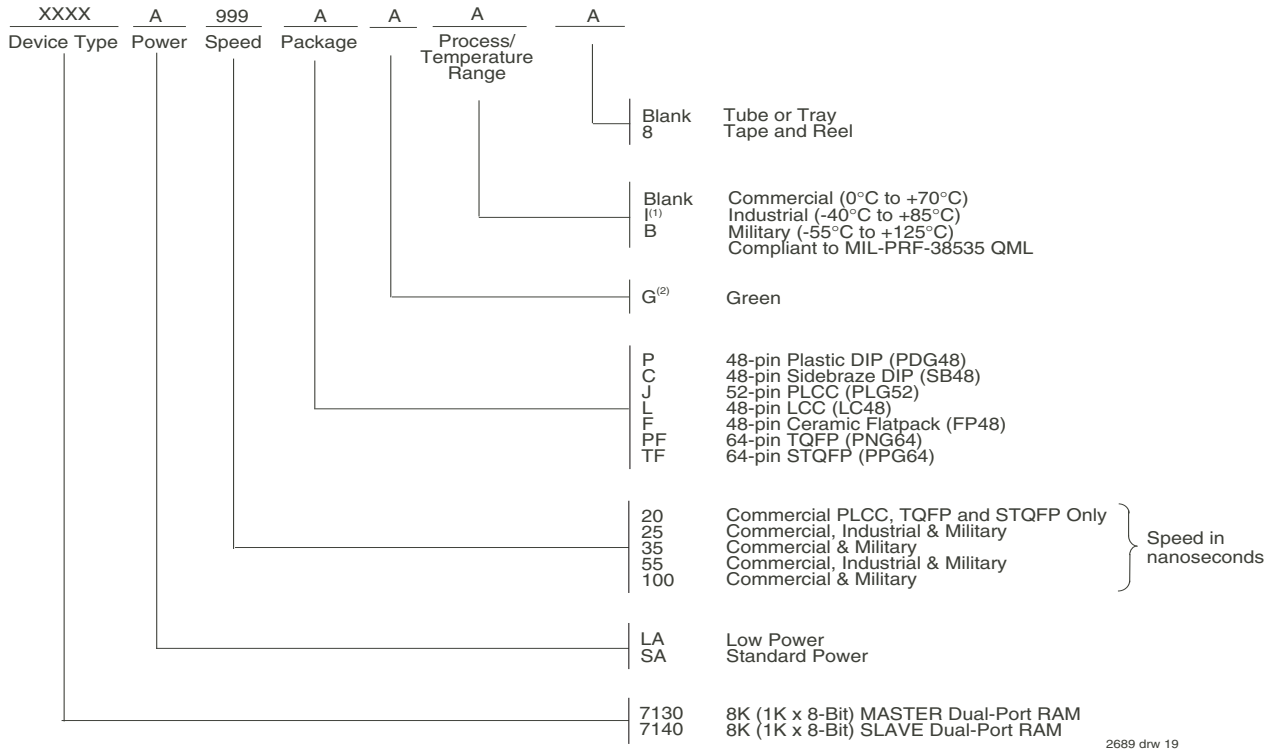



**Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7130 (Master) and IDT7140 (Slave)RAMs.**

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The $\overline{BUSY}$ arbitration, on a Master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a $\overline{BUSY}$ flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

# Ordering Information




**NOTES**:

1. Contact your local sales office for industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

LEAD FINISH (SnPb) parts are Obsolete excluding FP48, LC48 & SB48. Product Discontinuation Notice - PDN# SP-17-02
Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

## Orderable Part Information

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 20 | 7130LA20JG | PLG52 | PLCC | C |
| | 7130LA20JG8 | PLG52 | PLCC | C |
| | 7130LA20PFG | PNG64 | TQFP | C |
| | 7130LA20PFG8 | PNG64 | TQFP | C |
| | 7130LA20TFG | PPG64 | STQFP | C |
| | 7130LA20TFG8 | PPG64 | STQFP | C |
| 25 | 7130LA25JGI | PLG52 | PLCC | I |
| | 7130LA25JGI8 | PLG52 | PLCC | I |
| | 7130LA25L48B | LC48 | LCC | M |
| | 7130LA25PFGI | PNG64 | TQFP | I |
| | 7130LA25PFGI8 | PNG64 | TQFP | I |
| | 7130LA25TFGI | PPG64 | STQFP | I |
| 35 | 7130LA35C | SB48 | SB | C |
| | 7130LA35CB | SB48 | SB | M |
| | 7130LA35FB | FP48 | FPACK | M |
| | 7130LA35L48B | LC48 | LCC | M |
| | 7130LA35PDG | PDG48 | PDIP | C |
| 55 | 7130LA55C | SB48 | SB | C |
| | 7130LA55CB | SB48 | SB | M |
| | 7130LA55FB | FP48 | FPACK | M |
| | 7130LA55L48B | LC48 | LCC | M |
| | 7130LA55PDGI | PDG48 | PDIP | I |
| 100 | 7130LA100C | SB48 | SB | C |
| | 7130LA100CB | SB48 | SB | M |
| | 7130LA100L48B | LC48 | LCC | M |
| | 7130LA100PDG | PDG48 | PDIP | C |

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 25 | 7130SA25L48B | LC48 | LCC | M |
| 35 | 7130SA35C | SB48 | SB | C |
| | 7130SA35CB | SB48 | SB | M |
| | 7130SA35L48B | LC48 | LCC | M |
| 55 | 7130SA55C | SB48 | SB | C |
| | 7130SA55CB | SB48 | SB | M |
| | 7130SA55L48B | LC48 | LCC | M |
| 100 | 7130SA100C | SB48 | SB | C |
| | 7130SA100CB | SB48 | SB | M |
| | 7130SA100L48B | LC48 | LCC | M |

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 20 | 7140LA20JG | PLG52 | PLCC | C |
| | 7140LA20JG8 | PLG52 | PLCC | C |
| 25 | 7140LA25PFG | PNG64 | TQFP | C |
| | 7140LA25PFG8 | PNG64 | TQFP | C |
| 35 | 7140LA35CB | SB48 | SB | M |
| | 7140LA35FB | FP48 | FPACK | M |
| | 7140LA35L48B | LC48 | LCC | M |
| | 7140LA35PDG | PDG48 | PDIP | C |
| 55 | 7140LA55CB | SB48 | SB | M |
| | 7140LA55L48B | LC48 | LCC | M |
| 100 | 7140LA100CB | SB48 | SB | M |
| | 7140LA100L48B | LC48 | LCC | M |
| | 7140LA100PDG | PDG48 | PDIP | C |

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 35 | 7140SA35CB | SB48 | SB | M |
| | 7140SA35L48B | LC48 | LCC | M |
| 55 | 7140SA55CB | SB48 | SB | M |
| | 7140SA55L48B | LC48 | LCC | M |
| 100 | 7140SA100CB | SB48 | SB | M |

# Datasheet Document History

| | | |
|---|---|---|
| 03/15/99: | | Initiated datasheet document history |
| | | Converted to new format |
| | | Cosmetic and typographical corrections |
| | Pages 2 and 3 | Added additional notes to pin configurations |
| 06/08/99: | | Changed drawing format |
| 08/02/99: | Page 2 | Corrected package number in note 3 |
| 09/29/99: | Page 2 | Fixed pin 1 in DIP pin configuration |
| 11/10/99: | Page 1 & 18 | Replaced IDT logo |
| 06/23/00: | Page 4 | Increased storage temperature parameters |
| | | Clarified $T_A$ parameter |
| | Page 5 | DC Electrical parameters–changed wording from "open" to "disabled" |
| | Page 10 | Changed ±500mV to 0mV in notes |
| 01/08/02: | Page 1 | Added Ceramic Flatpack to 48-pin package offerings |
| | Page 2 & 3 | Added date revision to pin configurations |
| | Page 4, 5, 8, 10, 12,14 & 15 | Removed industrial temp option footnote from all tables |
| 01/08/02: | Page 5, 8, 10, 12, & 14 | Added industrial temp for 25ns to DC & AC Electrical Characteristics |
| | Page 5, 8, 10, 12, & 14 | Removed industrial temp for 35ns to DC & AC Electrical Characteristics |
| | Page 18 | Added industrial temp for 25ns and removed industrial temp for 35ns in ordering information |
| | | Updated industrial temp option footnote |
| | Page 1 & 19 | Replaced IDT TM logo with IDT ® logo |
| 01/11/06: | Page 1 | Added green availability to features |
| | Page 18 | Added green indicator to ordering information |
| | Page 1 & 19 | Replaced old IDT TM with new IDT TM logo |
| 04/14/06: | Page 18 | Added "PDG" footnote to the ordering information |
| 10/21/08: | Page 18 | Removed "IDT" from orderable part number |
| 01/21/13: | Page 2 | Added L48-1 package and F48-1 package pin configurations with corresponding foot notes |
| | Page 13, 18, 19 & 20 | Typo/corrections |
| | Page 20 | Added T & Reel indicator to ordering information |
| 05/20/16: | Page 2 | Split the F48 and L48 pin configuration, creating two separate pin configurations: F48 pin ceramic flatpack rotated 90 degrees counterclockwise, removed footnote 5 reference and L48 LCC rotated 90 degrees clockwise to reflect pin 1 orientation and added dot at pin 1, removed footnote 5 reference |
| | Page 3 | P48 plastic DIP and C48 sidebrazed DIP, removed half moon and to reflect pin 1 orientation added dot at pin 1 |
| | Page 4 | J52 PLCC rotated 90 degrees clockwise to reflect pin 1 orientation added dot at pin 1, removed footnote 5 reference |
| | Page 5 | PN64 TQFP and PP64 STQFP, chamfer removed, rotated 90 degrees counterclockwise to reflect pin 1 orientation and added dot at pin 1, removed footnote 5 reference |
| | Page 20 | All incidences of -1 , -2 have been removed from the datasheet |
| 02/13/18: | | Product Discontinuation Notice - PDN# SP-17-02 |
| | | Last time buy expires June 15, 2018 |
| 07/12/21: | Page 1 - 23 | Rebranded as Renesas datasheet |
| | Page 1 & 21 | Deleted obsolete Industrial speed grade for 100ns |
| | Page 2, 3, 4 & 5 | Updated package codes |
| | Page 21 | Added Orderable Part Information tables |

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