

# 74ABT245

Octal transceiver with direction pin; 3-state

Rev. 5 — 9 July 2021

Product data sheet

## 1. General description

The 74ABT245 is an 8-bit transceiver with 3-state outputs. The device features an output enable ( $\overline{OE}$ ) and send/receive (DIR) for direction control. A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

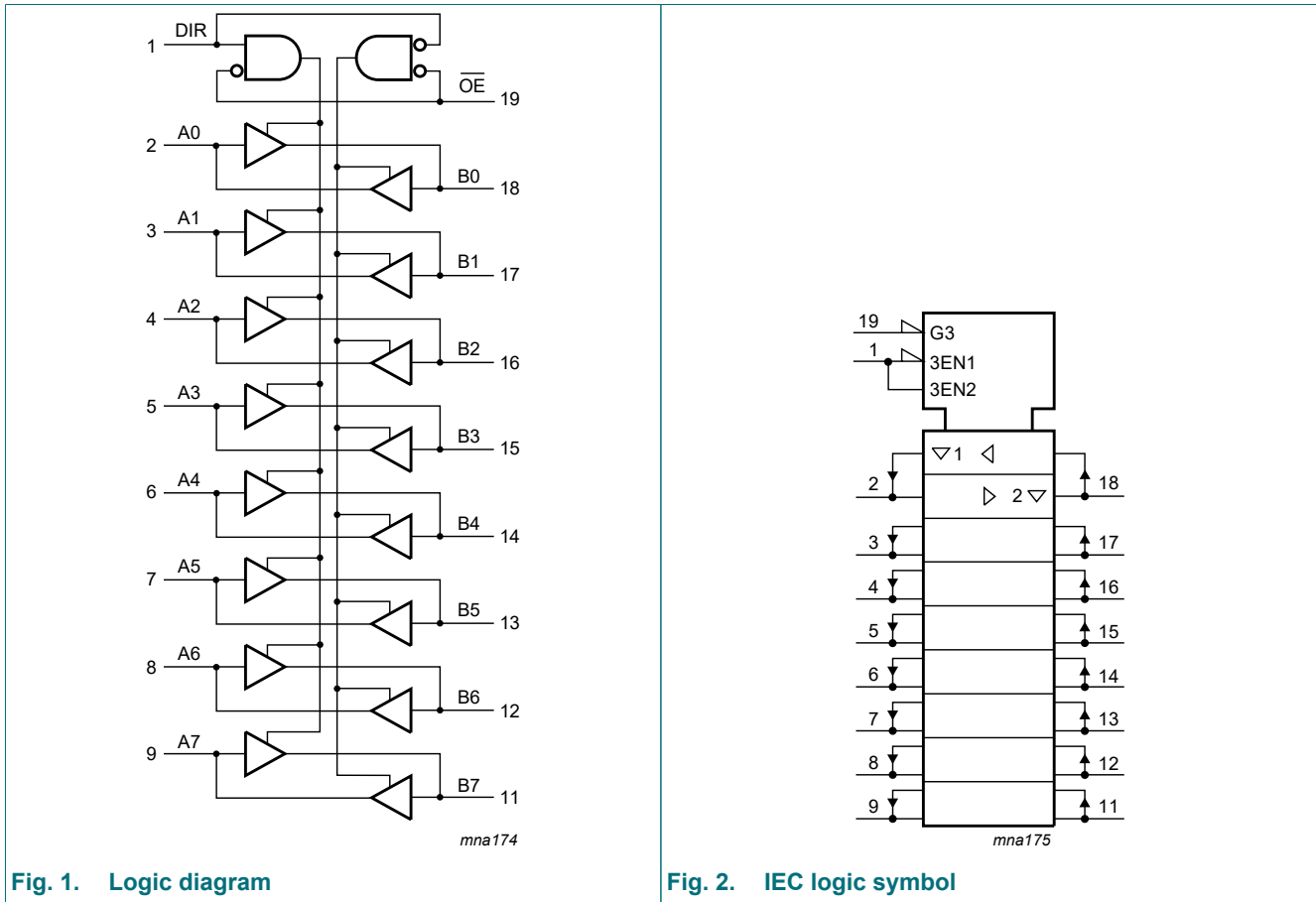
- Octal bidirectional bus interface
- 3-State buffers
- Supply voltage range from 4.5 to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Output capability: +64 mA/–32 mA
- Power-up 3-State
- Live insertion/extraction permitted
- Inputs are disabled during 3-state mode
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

## 3. Ordering information

Table 1. Ordering information

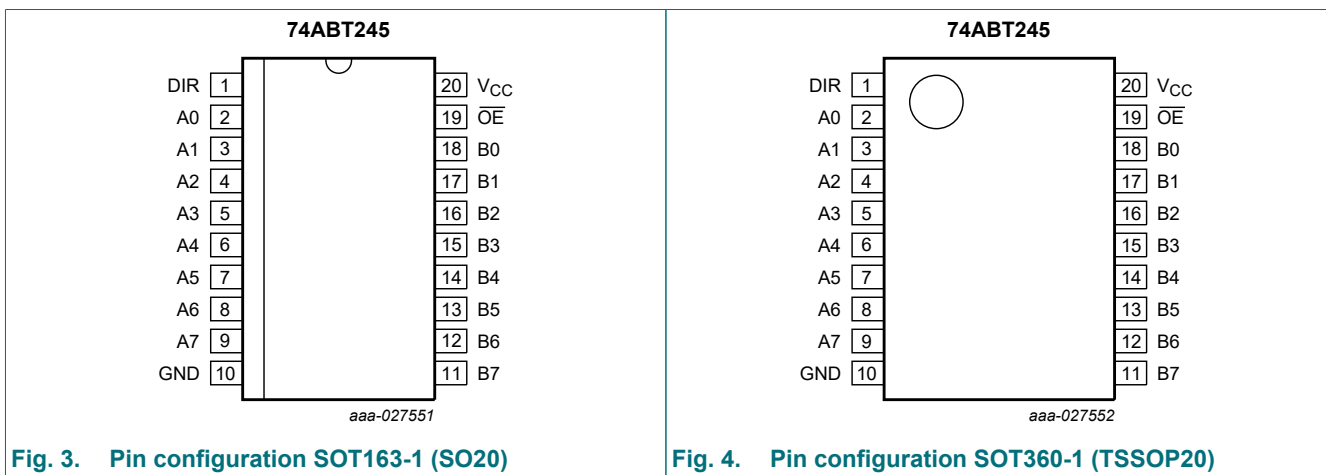
Type number	Package			Version
	Temperature range	Name	Description	
74ABT245D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ABT245PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

### 4. Functional diagram



### 5. Pinning information

#### 5.1. Pinning



## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control input
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
$\overline{OE}$	19	output enable input (active LOW)
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

Input		Input/output	
$\overline{OE}$	DIR	An	Bn
L	L	output An = Bn	input
L	H	input	output Bn = An
H	X	Z	Z

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage	[1]	-1.2	+7.0	V
V <sub>O</sub>	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+5.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-18	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
T <sub>j</sub>	junction temperature	[2]	-	150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$I_{OH}$	HIGH-level output current		-	-	-32	mA
$I_{OL}$	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = 25\text{ °C}$			$T_{amb} = -45\text{ °C to }+85\text{ °C}$		Unit
			Min	Typ	Max	Min	Max	
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5\text{ V}; I_{IK} = -18\text{ mA}$	-1.2	-0.9	-	-1.2	-	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	2.0	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 4.5\text{ V}; V_I = V_{IL}\text{ or }V_{IH}$						
		$I_{OH} = -3\text{ mA}$	2.5	2.9	-	2.5	-	V
		$I_{OH} = -32\text{ mA}$	2.0	2.4	-	2.0	-	V
		$V_{CC} = 5.0\text{ V}; V_I = V_{IL}\text{ or }V_{IH}$						
		$I_{OH} = -3\text{ mA}$	3.0	3.4	-	3.0	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 4.5\text{ V}; V_I = V_{IL}\text{ or }V_{IH}; I_{OL} = 64\text{ mA}$	-	0.42	0.55	-	0.55	V
$I_I$	input leakage current	Control pins; $V_{CC} = 5.5\text{ V}; V_I = \text{GND or }5.5\text{ V}$	-	$\pm 0.01$	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
		Data pins; $V_{CC} = 5.5\text{ V}; V_I = \text{GND or }5.5\text{ V}$	-	$\pm 5$	$\pm 100$	-	$\pm 100$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}; V_O\text{ or }V_I \leq 4.5\text{ V}$	-	$\pm 5.0$	$\pm 100$	-	$\pm 100$	$\mu\text{A}$
$I_{O(pu/pd)}$	power-up/ power-down output current	$V_{CC} = 2.0\text{ V}; V_O = 0.5\text{ V}; V_I = \text{GND or }V_{CC}; \overline{OE} = \text{don't care}$ [1]	-	$\pm 5.0$	$\pm 50$	-	$\pm 50$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_{CC} = 5.5\text{ V}; V_I = V_{IL}\text{ or }V_{IH}$						
		output HIGH-state at $V_O = 2.7\text{ V}$	-	5.0	50	-	50	$\mu\text{A}$
		output LOW-state at $V_O = 0.5\text{ V}$	-	-5.0	-50	-	-50	$\mu\text{A}$
$I_{CEX}$	output high leakage current	$V_{CC} = 5.5\text{ V}; V_O = 5.5\text{ V}; V_I = \text{GND or }V_{CC}$	-	5.0	50	-	50	$\mu\text{A}$
$I_O$	output current	$V_{CC} = 5.5\text{ V}; V_O = 2.5\text{ V}$ [2]	-40	-100	-180	-40	-180	mA

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -45 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>						
		outputs HIGH-state	-	50	250	-	250	μA
		outputs LOW-state	-	24	30	-	30	mA
		outputs disabled	-	50	250	-	250	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 5.5 V						
		outputs enabled; one input at 3.4 V and other inputs at V <sub>CC</sub> or GND [3]	-	0.5	1.5	-	1.5	mA
		outputs disabled; one data input at 3.4 V and other inputs at V <sub>CC</sub> or GND [3]	-	50	250	-	250	μA
		outputs disabled; one enable input at 3.4 V and other inputs at V <sub>CC</sub> or GND [3]	-	0.5	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance	DIR; $\overline{OE}$ ; V <sub>I</sub> = 0 V or V <sub>CC</sub>	-	4	-	-	-	pF
C <sub>I/O</sub>	input/output capacitance	outputs disabled; V <sub>O</sub> = 0 V or V <sub>CC</sub>	-	7	-	-	-	pF

[1] This parameter is valid for any V<sub>CC</sub> between 0 V and 2.1 V, with a transition time of up to 10 ms.

From V<sub>CC</sub> = 2.1 V to V<sub>CC</sub> = 5 V ± 10 % a transition time of up to 100 μs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

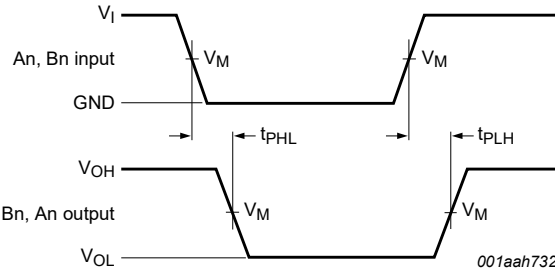
## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C; V <sub>CC</sub> = 5.0 V			T <sub>amb</sub> = -40 °C to 85 °C; V <sub>CC</sub> = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub> ; see Fig. 5	1.0	2.2	4.1	1.0	4.6	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub> ; see Fig. 5	1.0	2.9	4.2	1.0	4.6	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	$\overline{OE}$ to A <sub>n</sub> or B <sub>n</sub> ; see Fig. 6	1.3	3.0	4.8	1.3	5.3	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	$\overline{OE}$ to A <sub>n</sub> or B <sub>n</sub> ; see Fig. 6	2.3	4.0	5.8	2.3	6.3	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	$\overline{OE}$ to A <sub>n</sub> or B <sub>n</sub> ; see Fig. 6	1.0	4.7	6.2	1.0	7.2	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	$\overline{OE}$ to A <sub>n</sub> or B <sub>n</sub> ; see Fig. 6	1.0	4.1	5.8	1.0	6.3	ns

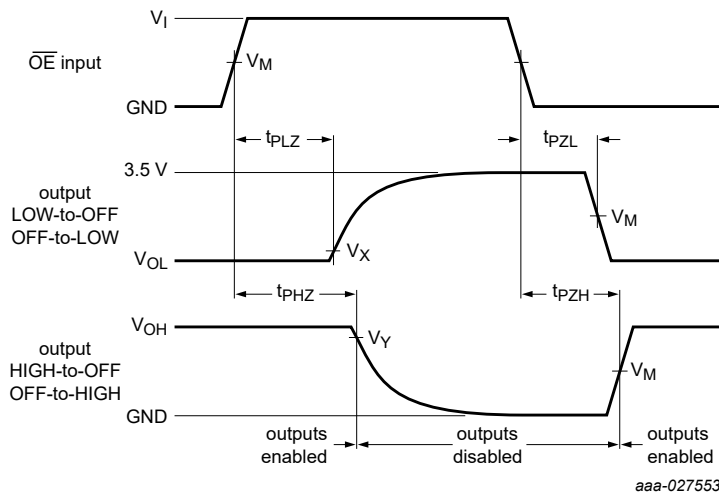
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output drop that occur with the output load.

Fig. 5. Input (An or Bn) to output (Bn or An) propagation delays



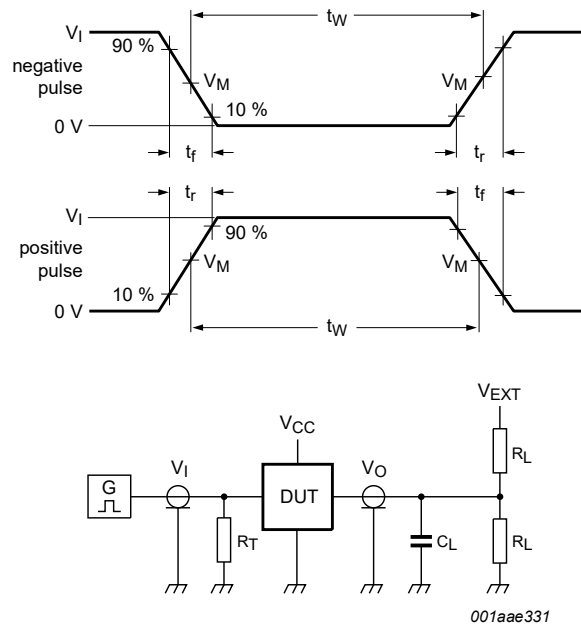
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output drop that occur with the output load.

Fig. 6. 3-state output enable and disable propagation delays

Table 8. Measurement points

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = Test voltage for switching times.

**Fig. 7. Test circuit for measuring switching times**

**Table 9. Test data**

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
3.0 V	$\leq 1$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	7 V	open

### 11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

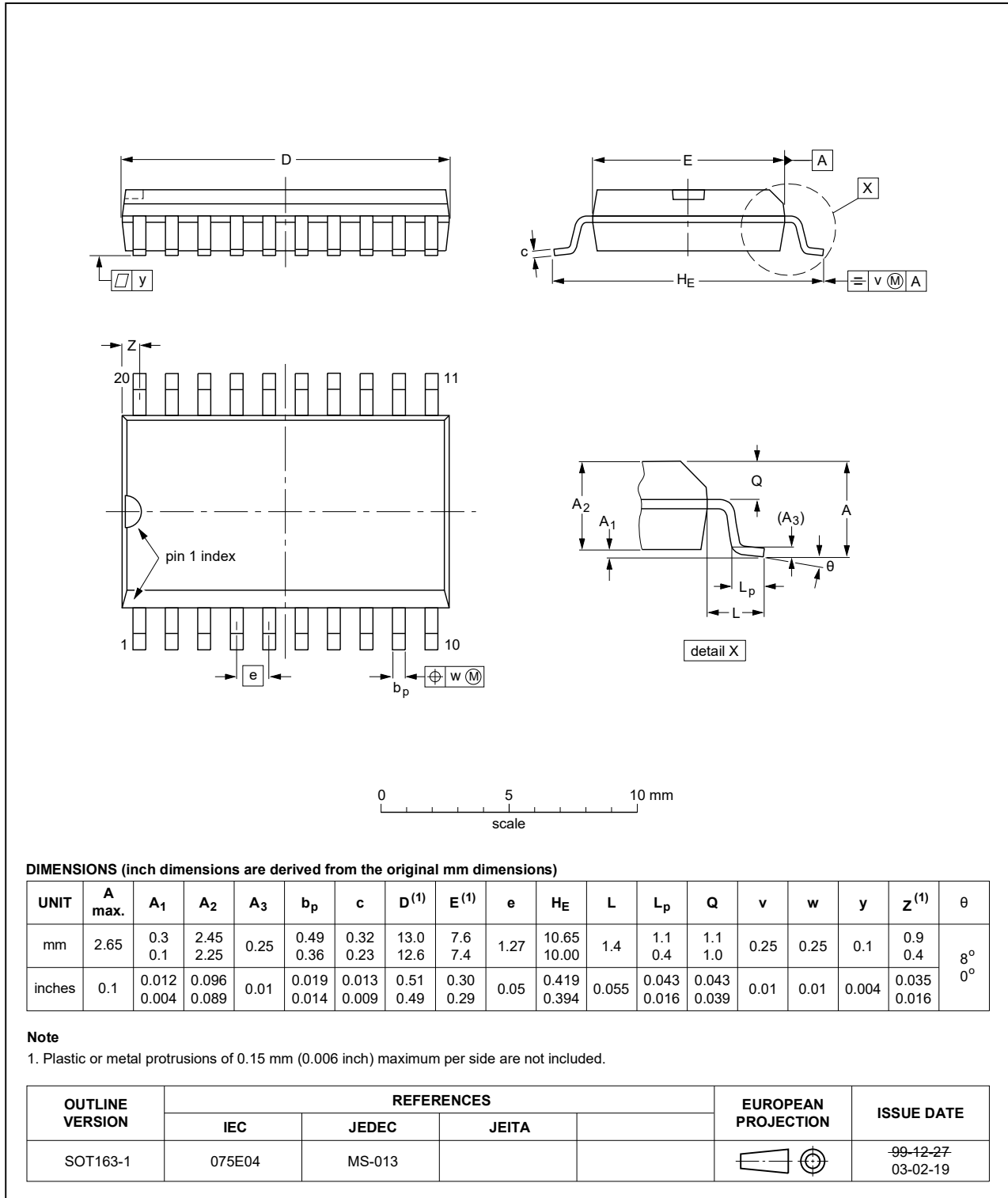


Fig. 8. Package outline SOT163-1 (SO20)



TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

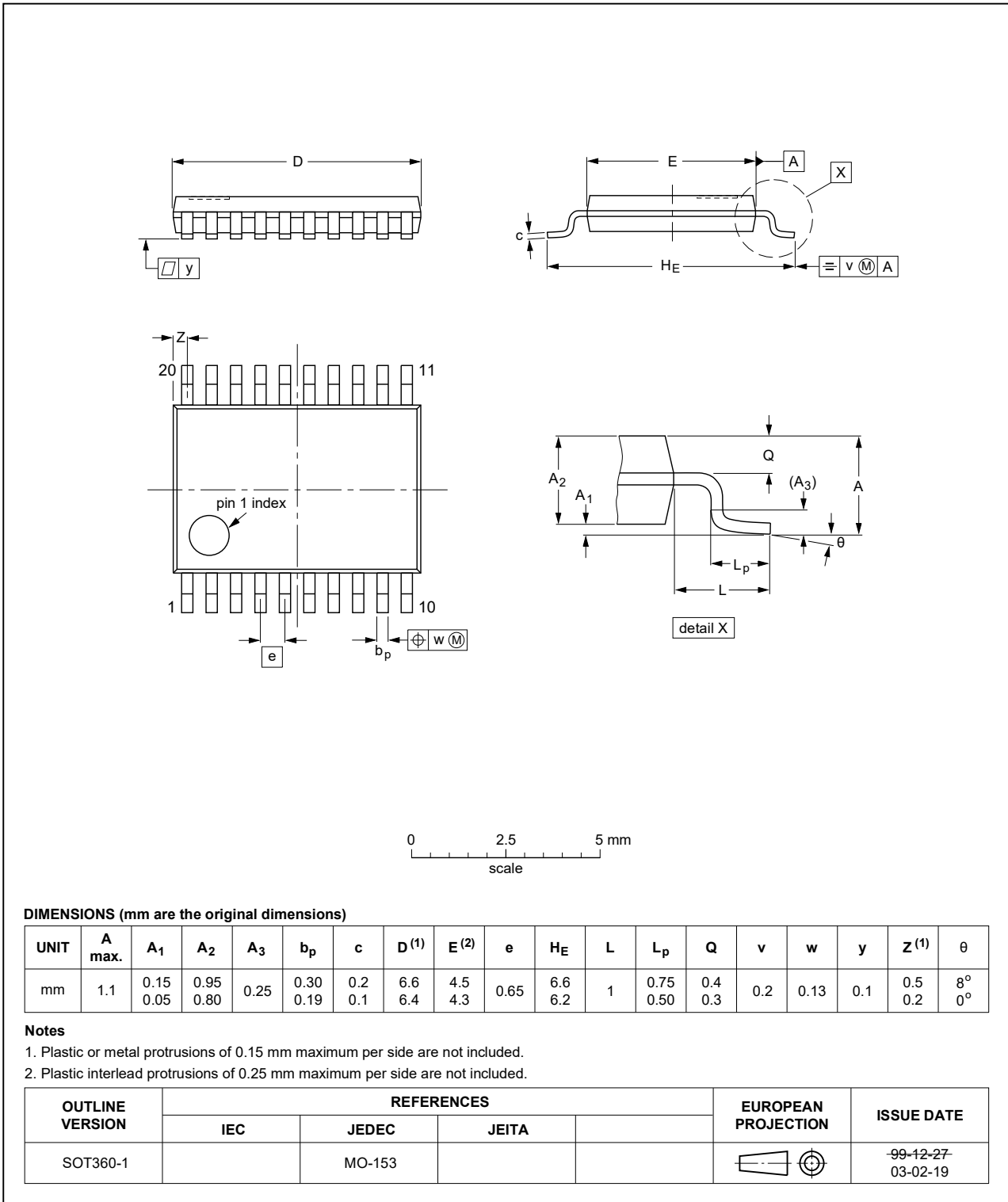


Fig. 9. Package outline SOT360-1 (TSSOP20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT245 v.5	20210709	Product data sheet	-	74ABT245 v.4
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>• Type number 74ABT245DB (SOT339-1 / SSOP20) removed.</li> </ul>			
74ABT245 v.4	20171006	Product data sheet	-	74ABT245 v.3
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74ABT245 v.3	20030206	Product data sheet	ECN 853-1447 29305	74ABT245 v.2
Modifications:	<ul style="list-style-type: none"> <li>• Delete all references to N package. DIP20 package option discontinued.</li> </ul>			
74ABT245 v.2	19980116	Product specification	ECN 853-1447 18867	74ABT245 v.1
74ABT245 v.1	19960910	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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