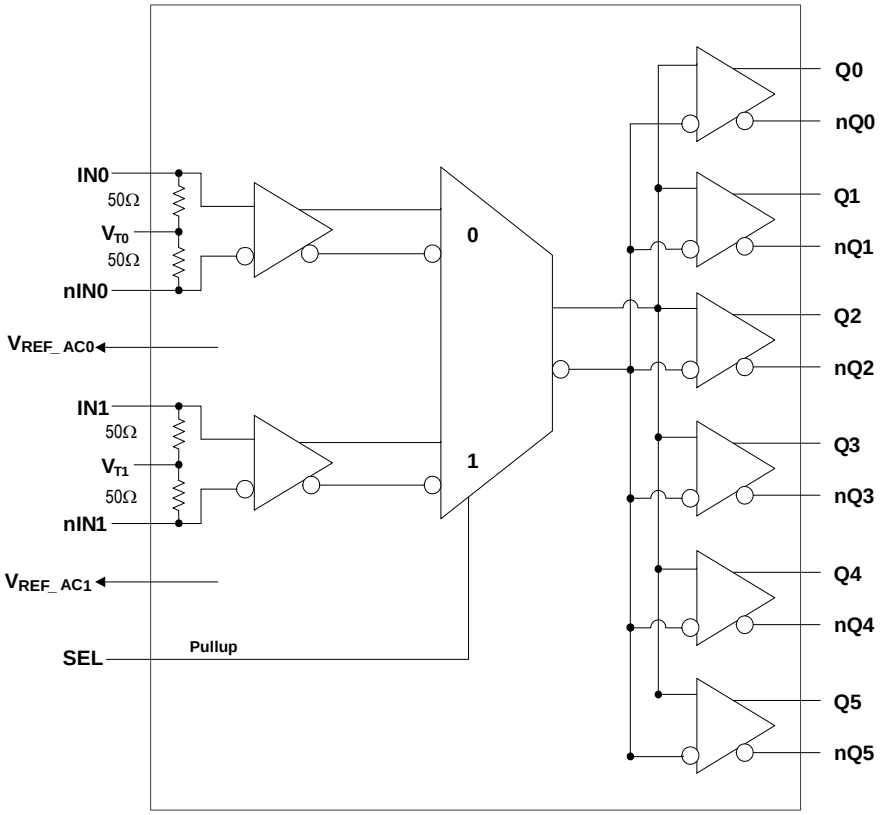
General Description

The 8S58035I is a high speed 2-to-6 Differential-to-LVPECL Fanout Buffer. The 8S58035I is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fiber Channel. The internally terminated differential inputs and V_{REF_AC} pins allow other differential signal families such as LVDS, LVHSTL and CML to be easily interfaced to the input with minimal use of external components. The device also has a 2:1 MUX input, allowing for easy selection between two clock reference sources. The 8S58035I is packaged in a small 5mm x 5mm 32-pin VFQFN package which makes it ideal for use in space-constrained applications.

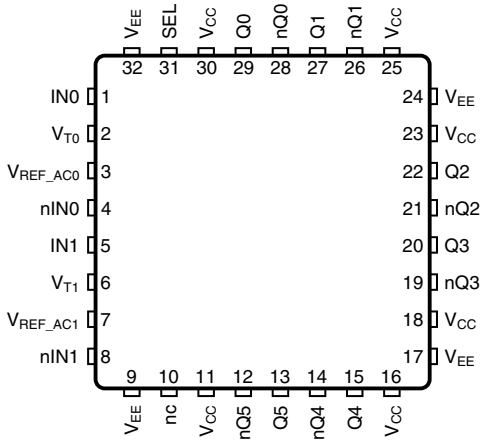
Features

- Six LVPECL outputs
- INx, nINx inputs can accept the following differential input levels: LVPECL, LVDS, CML
- 50Ω internal input termination to V_T
- Two selectable differential input pairs
- Maximum output frequency: 3.2GHz
- Output Skew: 45ps (maximum)
- Part-to-Part Skew: 200ps (maximum)
- Additive phase jitter, RMS: 47fs (typical), (f_{REF} = 622.08MHz, 12kHz - 20MHz, V_{CC} = 3.3V)
- Propagation Delay: 580ps (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 2.5V±5%, 3.3V±10%, V_{EE} = 0V
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



8S58035I

32-Lead VFQFN
5mm x 5mm x 0.925mm package body
3.15mm x 3.15mm Epad Size
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 5	IN0, IN1	Input		Non-inverting differential LVPECL clock inputs. R_T = 50Ω termination to V_T.
2, 6	V_{T0}, V_{T1}	Input		Termination inputs.
3, 7	V_{REF_AC0}, V_{REF_AC1}	Output		Reference voltage for AC-coupled applications.
4, 8	nIN0, nIN1	Input		Inverting differential LVPECL clock inputs. R_T = 50Ω termination to V_T.
9, 17, 24, 32	V_{EE}	Power		Negative supply pins.
10	nc			No connect pin.
11, 16, 18, 23, 25, 30	V_{CC}	Power		Positive supply pins.
12, 13	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
14, 15	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
19, 20	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
21, 22	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
26, 27	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
28, 29	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.
31	SEL	Input	Pullup	Input select pin. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* refers to an internal input resistor. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3. SEL Function Table

SEL	Function
0	IN0, nIN0 input selected
1	IN, nIN1 input selected (default)

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Input Current, I_{IN} (IN0, nIN0, IN1, nIN1) V_T Current, I_{VT} V_{REF_AC} Input Sink/Source, I_{REF_AC}	±50mA ±100mA ±2mA
Package Thermal Impedance, θ_{JA}	42.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.375V to 3.6V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.6	V
I_{EE}	Power Supply Current				90	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 2.375V to 3.6V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{CC} = 3.6V	2.2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	V_{CC} = 3.6V	-0.3		0.8	V
I_{IH}	Input High Current	V_{CC} = V_{IN} = 3.6V			10	µA
I_{IL}	Input Low Current	V_{CC} = 3.6V, V_{IN} = 0V	-150			uA

Table 4C. Differential DC Characteristics, V_{CC} = 2.375V to 3.6V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{DIFF_IN}	Differential Input Resistance	IN0-to-nIN0 or IN1-to-nIN1		80	100	120	Ω
R_{IN}	Input Resistance	INx-to-V_{TX} or nINx-to-V_{TX}		40	50	60	Ω
V_{IH}	Input High Voltage	IN0, nIN0, IN1, nIN1		1.2		V_{CC}	V
V_{IL}	Input Low Voltage	IN0, nIN0, IN1, nIN1		0		V_{IH} – 0.15	V
V_{IN}	Input Voltage Swing; NOTE 1			0.15		1.4	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3		2.8	V
I_{IN}	Input Current; NOTE 2, 3	IN0, nIN0, IN1, nIN1				45	mA
V_{REF_AC}	Bias Voltage	V_{REF_AC0} or V_{REF_AC1}		V_{CC} - 1.4	V_{CC} – 1.3	V_{CC} – 1.2	V

NOTE 1: Refer to Parameter Measurement Information, *Input Voltage Swing diagram.*
NOTE 2: Guaranteed by design.
NOTE 3: Because of the internal termination R_{IN}, the input current I_{IN} will be determined by the voltages applied at INx, nINx and V_{Tx}. Observe the voltages applied to those pins so the input current does not exceed the maximum limit.

Table 4D. LVPECL DC Characteristics, V_{CC} = 2.375V to 3.6V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE1		V_{CC} - 1.05		V_{CC} - 0.85	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 1.9		V_{CC} - 1.6	V
V_{OUT}	Output Voltage Swing		0.55		1.0	mV
V_{DIFF_OUT}	Differential Output Voltage Swing		1.1		2.0	V

NOTE: Output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V

AC Electrical Characteristics

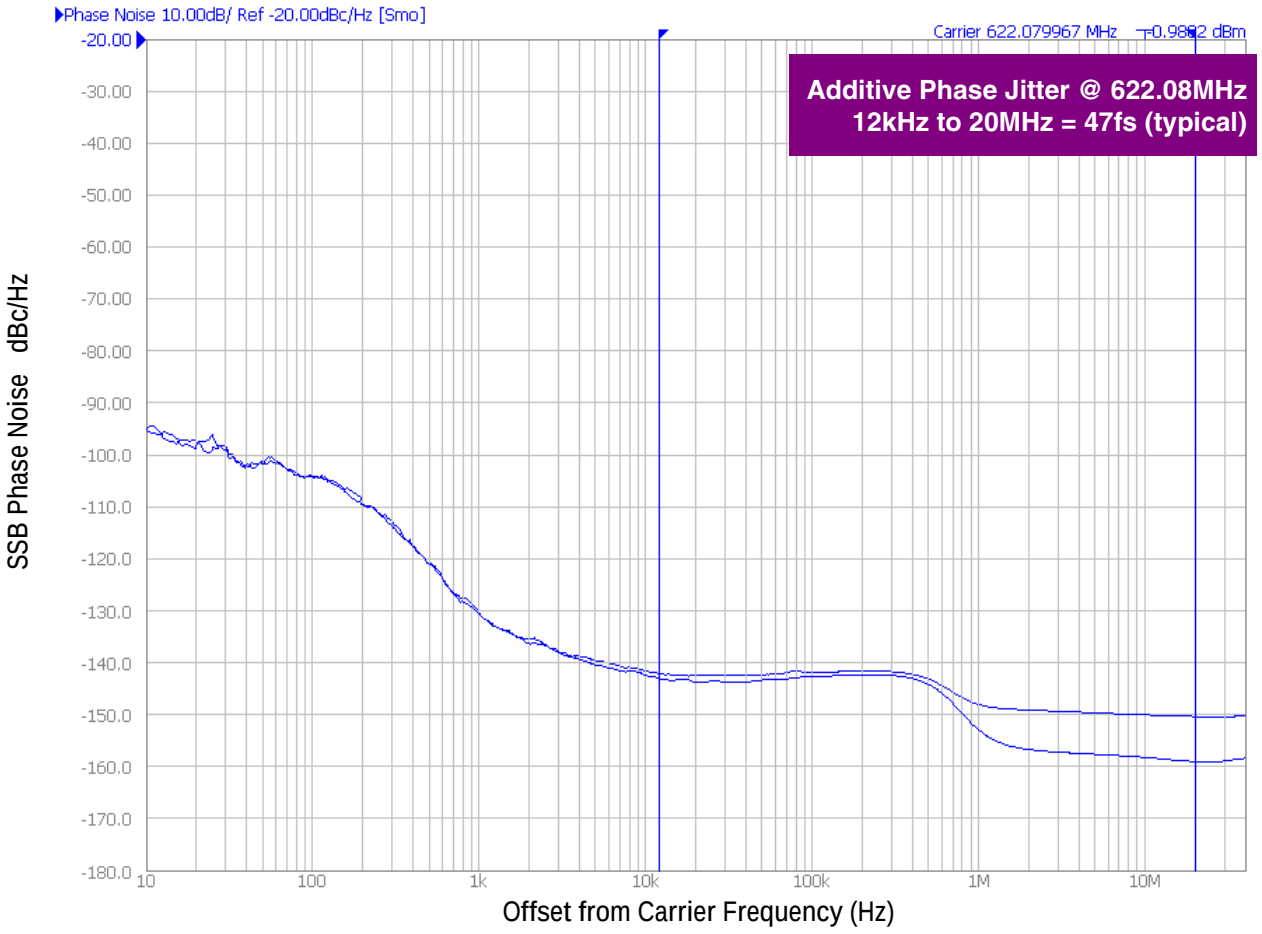
Table 5. AC Characteristics, V_{CC} = 2.375V to 3.6V, V_{EE} = 0V, T_A = -40°C to 85°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					3.2	GHz
t_{PD}	Propagation Delay; NOTE 1	INx to Qx		390	480	580	ps
tsk(o)	Output Skew; NOTE 2, 4					45	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					200	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section		622.08MHz, Integration Range: 12kHz to 20MHz		47		fs
t_R / t_F	Output Rise/Fall Time		20% - 80%	40		160	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters characterized at $f_{OUT} \leq$ 3.2GHz input signal, unless otherwise noted.
NOTE 1: Measured from the differential input crosspoint to the differential output crosspoint.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Additive Phase Jitter

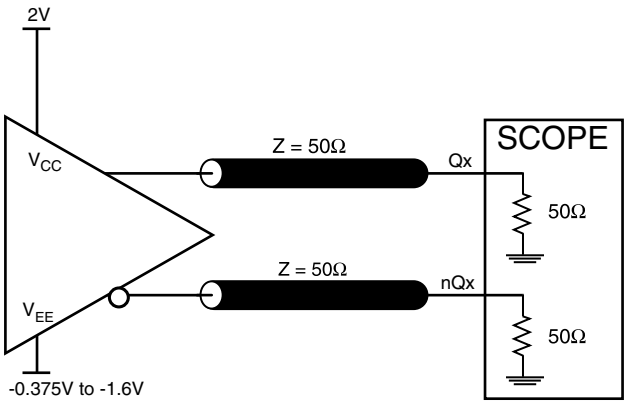
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



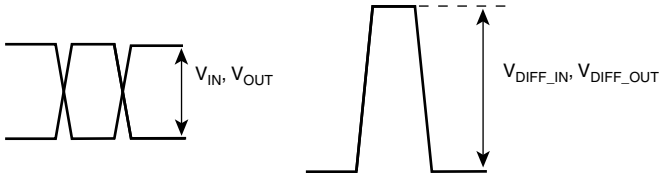
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Rohde & Schwarz SMA100A as the input source.

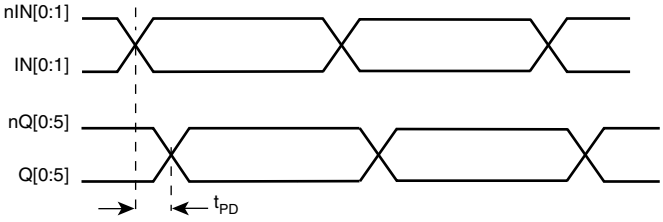
Parameter Measurement Information



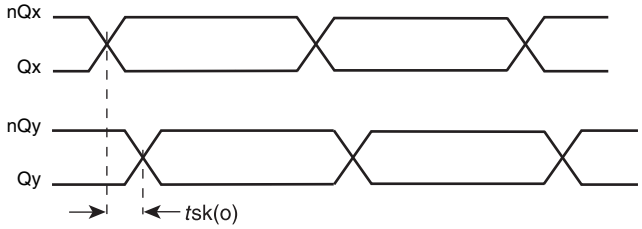
Output Load Test Circuit



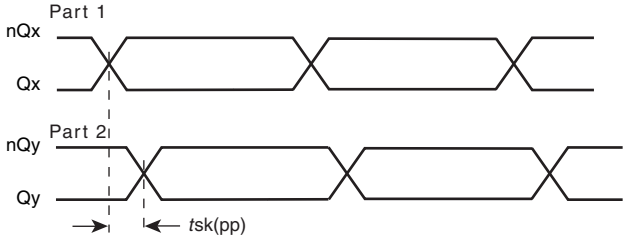
Single-ended & Differential Input/Output Swing



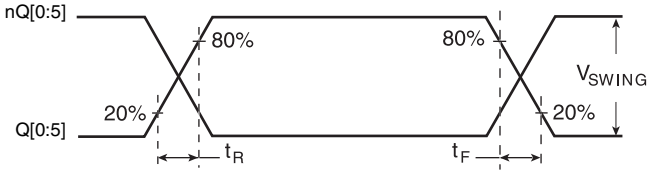
Propagation Delay



Output Skew



Part-to-Part Skew



Output Rise/Fall Time

Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

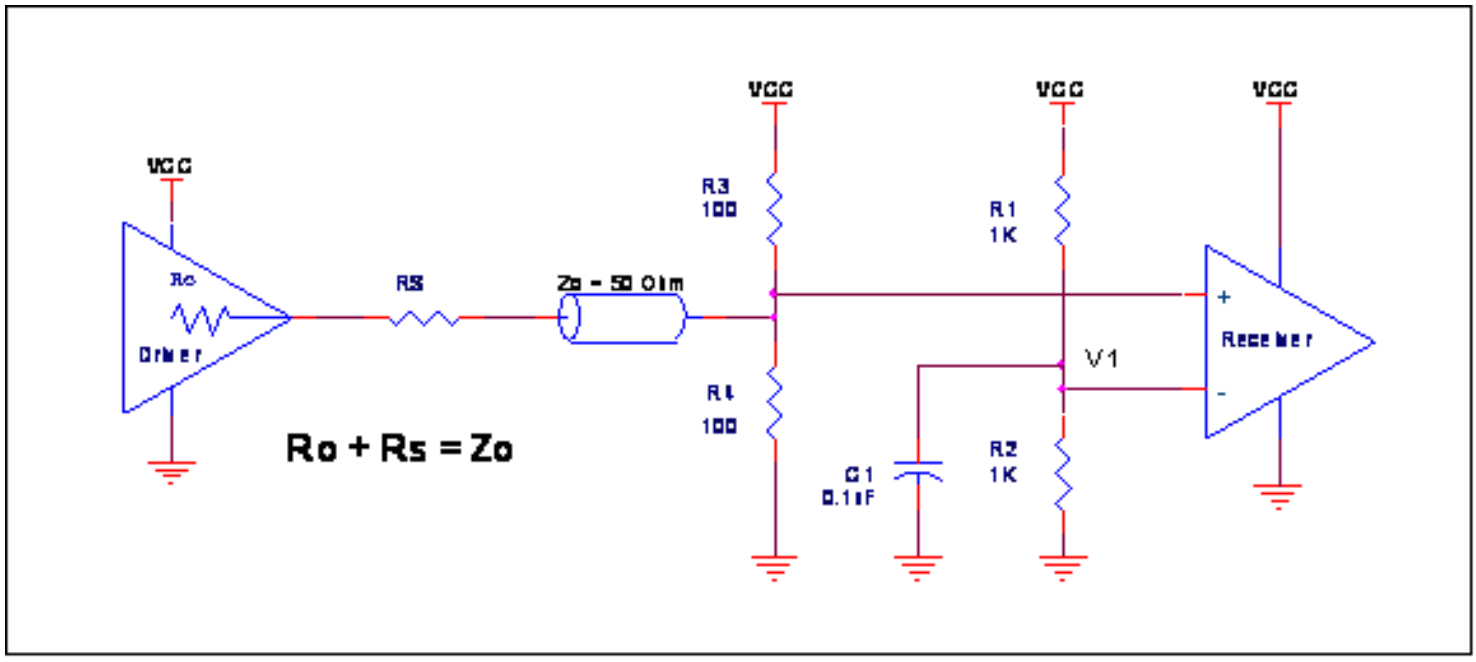


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

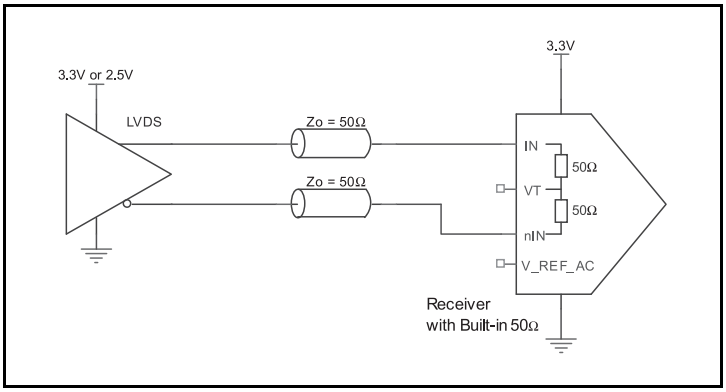


Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

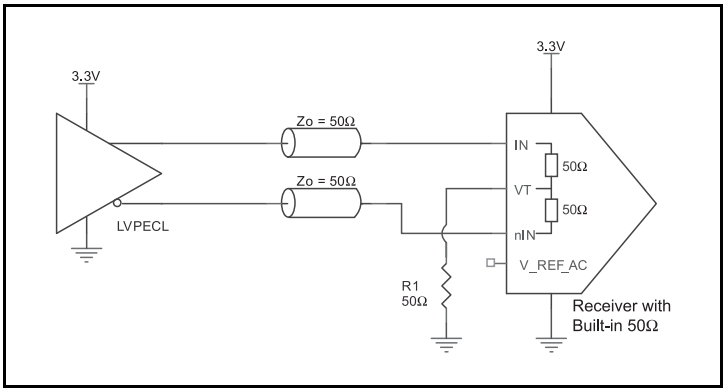


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

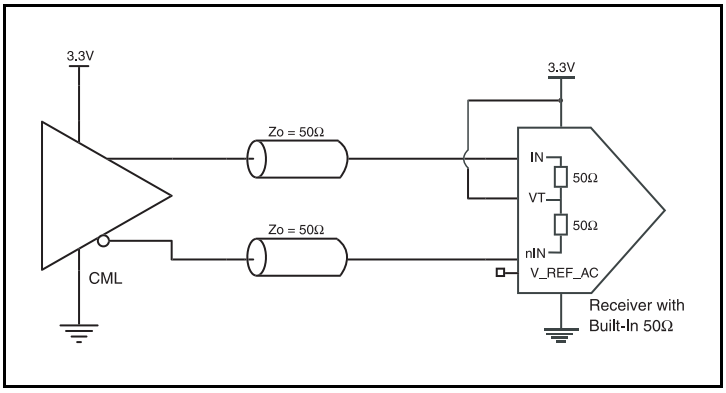


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

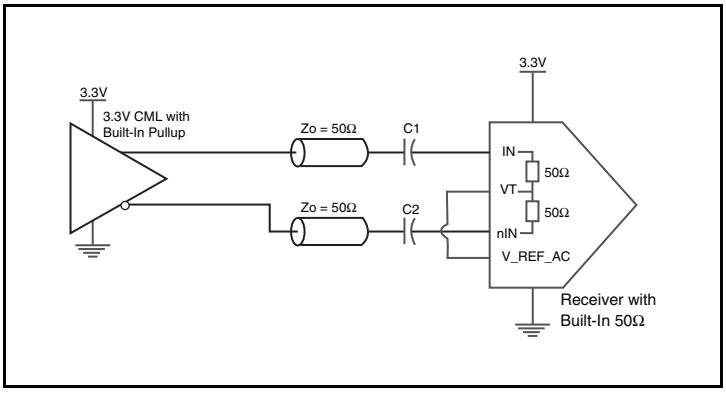


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 3A to 3D* show interface examples for the IN/nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

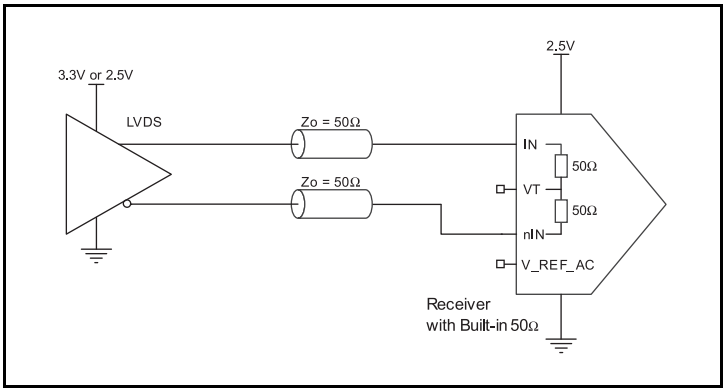


Figure 3A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

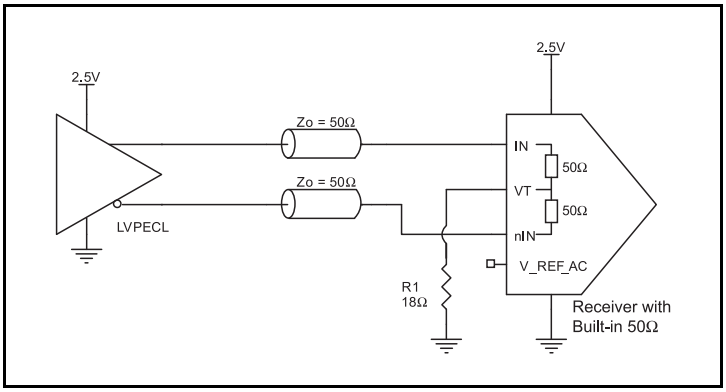


Figure 3B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

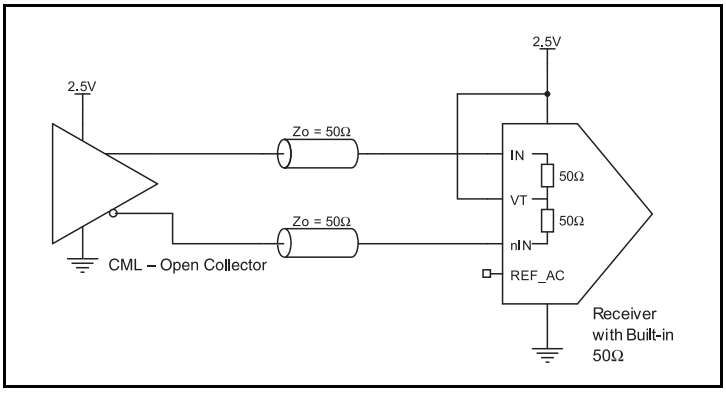


Figure 3C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

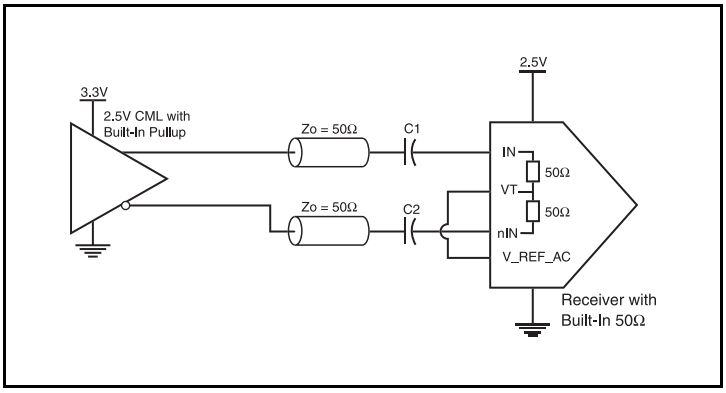


Figure 3D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

Recommendations for Unused Output Pins

Outputs:

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

2.5V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and complement of the unused input as shown in *Figure 4A.*

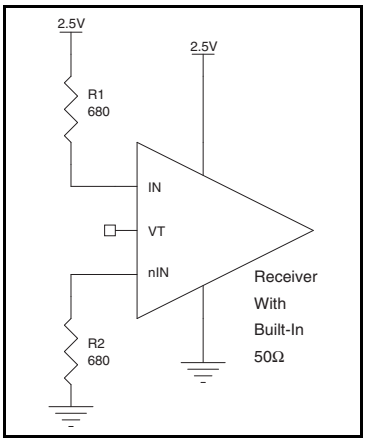


Figure 4A. Unused Input Handling

3.3V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and complement of the unused input as shown in *Figure 4B.*

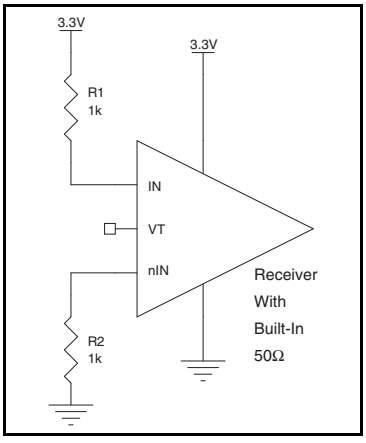


Figure 4B. Unused Input Handling

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

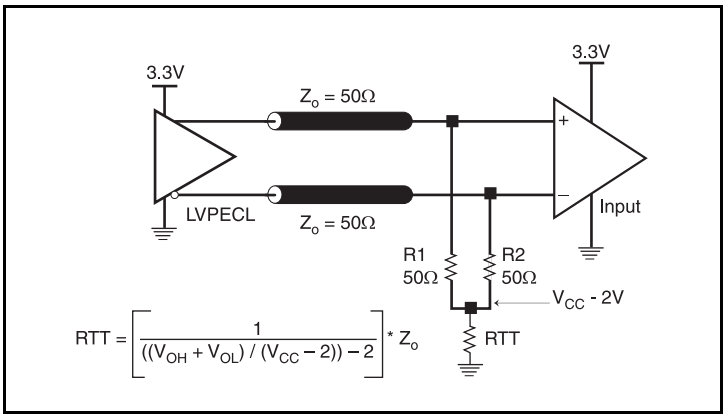


Figure 5A. 3.3V LVPECL Output Termination

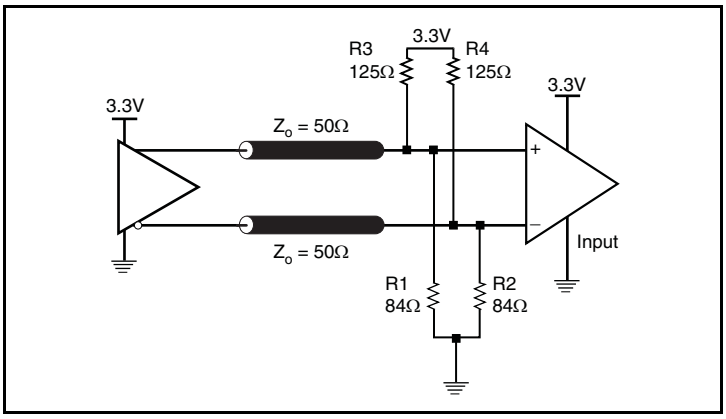


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

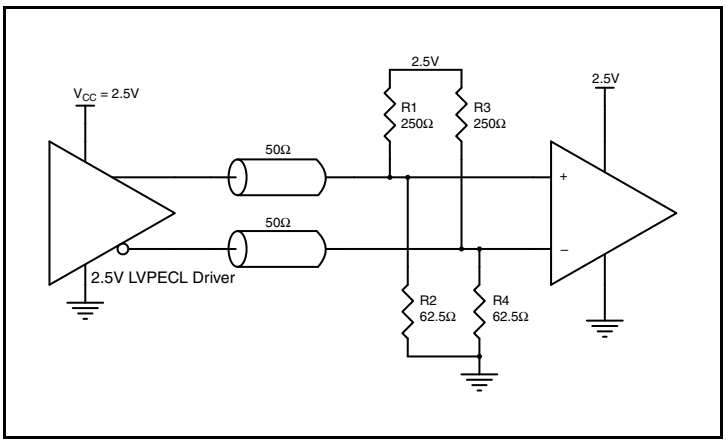


Figure 6A. 2.5V LVPECL Driver Termination Example

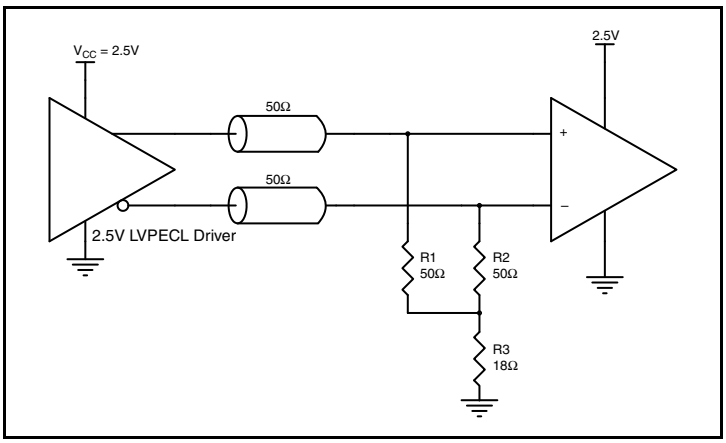


Figure 6B. 2.5V LVPECL Driver Termination Example

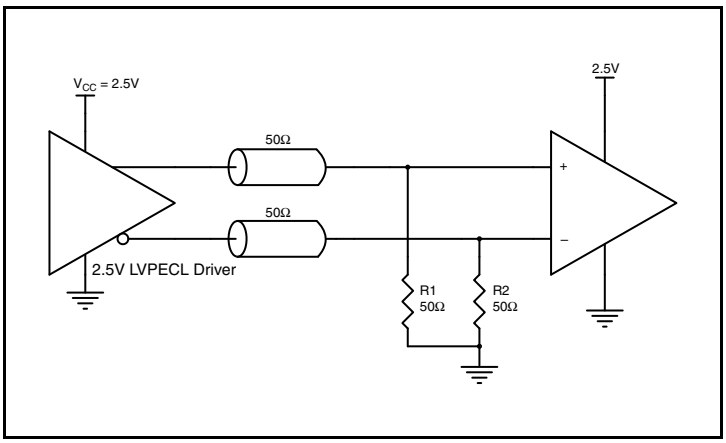


Figure 6C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 7.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

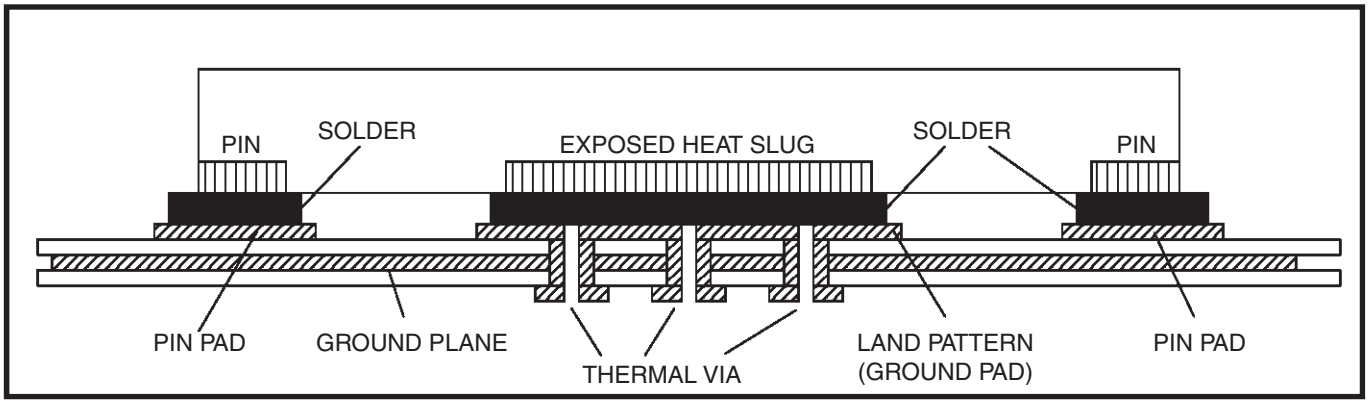


Figure 7. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8S58035I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8S58035I is the sum of the core power plus the output power dissipated due to loading.
The following is the power dissipation for V_{CC} = 3.6V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating output power dissipated due to loading.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.6V * 90mA = **324mW**
- Power $(outputs)_{MAX}$ = **32.35mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 32.35mW = **194.1mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX} = 2 * [(V_{IN\_MAX})^2 / (2 * R_{T\_MIN})] = 2 * [(1.4V)^2 / (2 * 40\Omega)]$ = **49mW**

Total Power$_{\_MAX}$ (3.6V, with all outputs switching) = 324mW + 194.1mW + 49mW**= 567.1mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.567W * 42.7°C/W = 109°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board.

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 7.*

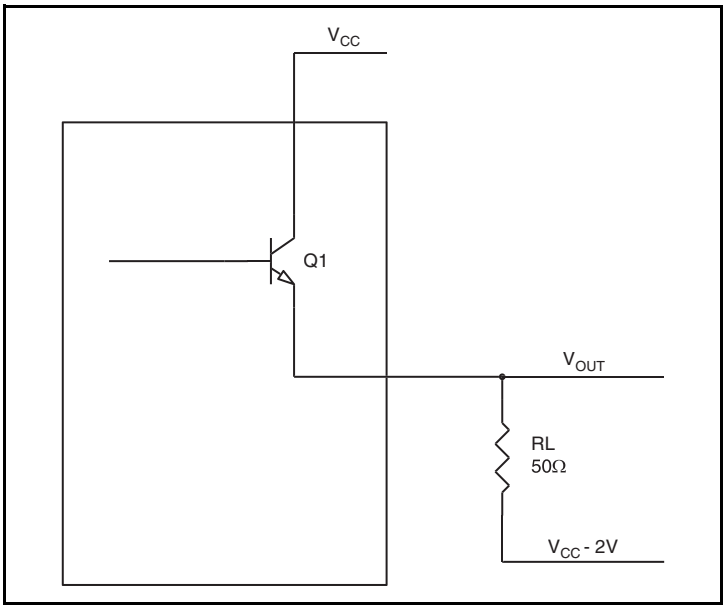


Figure 7. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage
of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CC_MAX} – 0.85V**
  ($V_{CC\_MAX} – V_{OH\_MAX}$) = **0.85V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CC_MAX} – 1.6V**
  ($V_{CC\_MAX} – V_{OL\_MAX}$) = **1.6V**

Pd_H is the power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.85V)/50Ω] * 0.85V =$ **19.55mW**

Pd_L = $[(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.6V)/50Ω] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.35mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

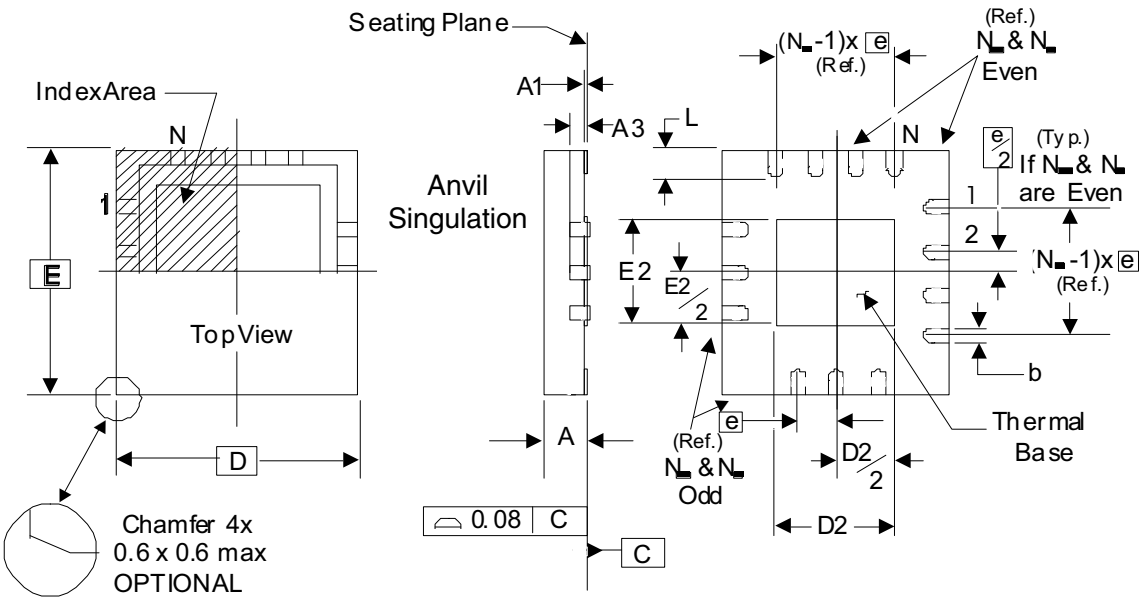
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

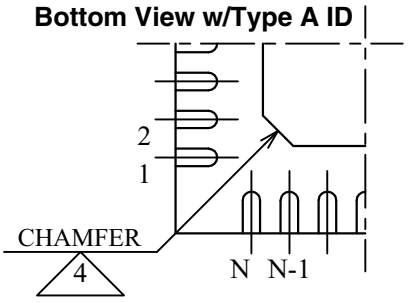
Transistor Count

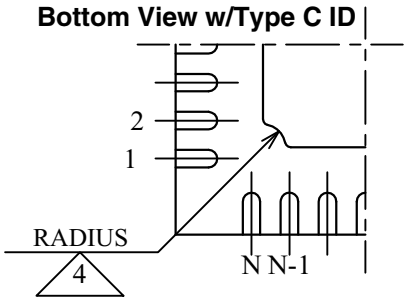
The transistor count for 8S58035I: 348

32 Lead VFQFN Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: This package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S58035AKILF	ICS58035AIL	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
8S58035AKILFT	ICS58035AIL	“Lead-Free” 32 Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History

Revision Date	Description of Change
February 5, 2016	▪ Removed ICS from the part number where needed. ▪ Updated header and footer.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.