Datasheet

DS000440

CMV20000

20MP CMOS Machine Vision Image Sensor

v2-00 • 2020-Feb-03

Content Guide

1 General Description

The CMV20000 is a global shutter CMOS image sensor with 5120 by 3840 pixels. The image array consists of 6.4 µm x 6.4 µm pipelined global shutter pixels, which allow exposure during read out while performing CDS operation. The image sensor has sixteen 12-bit digital LVDS outputs (serial). The image sensor also integrates a programmable gain amplifier and offset regulation. Each channel runs at 480 Mbps maximum which results in 30 fps frame rate at full resolution. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. A programmable on-board sequencer generates all internal exposure and read out timings. External triggering and exposure programming is possible. Extended optical dynamic range can be achieved by multiple integrated high dynamic range modes.

1.1 Key Benefits & Features

The benefits and features of CMV20000, 20MP CMOS Machine Vision Image Sensor, are listed below:

Figure 1:
Added Value of Using CMV20000

Benefits	Features
Capture fast moving objects	8T global shutter pixel with true Correlated Double Sampling (true-CDS)
Designed for high performance applications	Resolution of 5120 x 3840 at 30 frames per second
Capable of using standard optics	35 mm full frame optical format sensor

1.2 Applications

- Machine vision
- Video and broadcast
- High resolution display inspection
- Medical
- Scientific

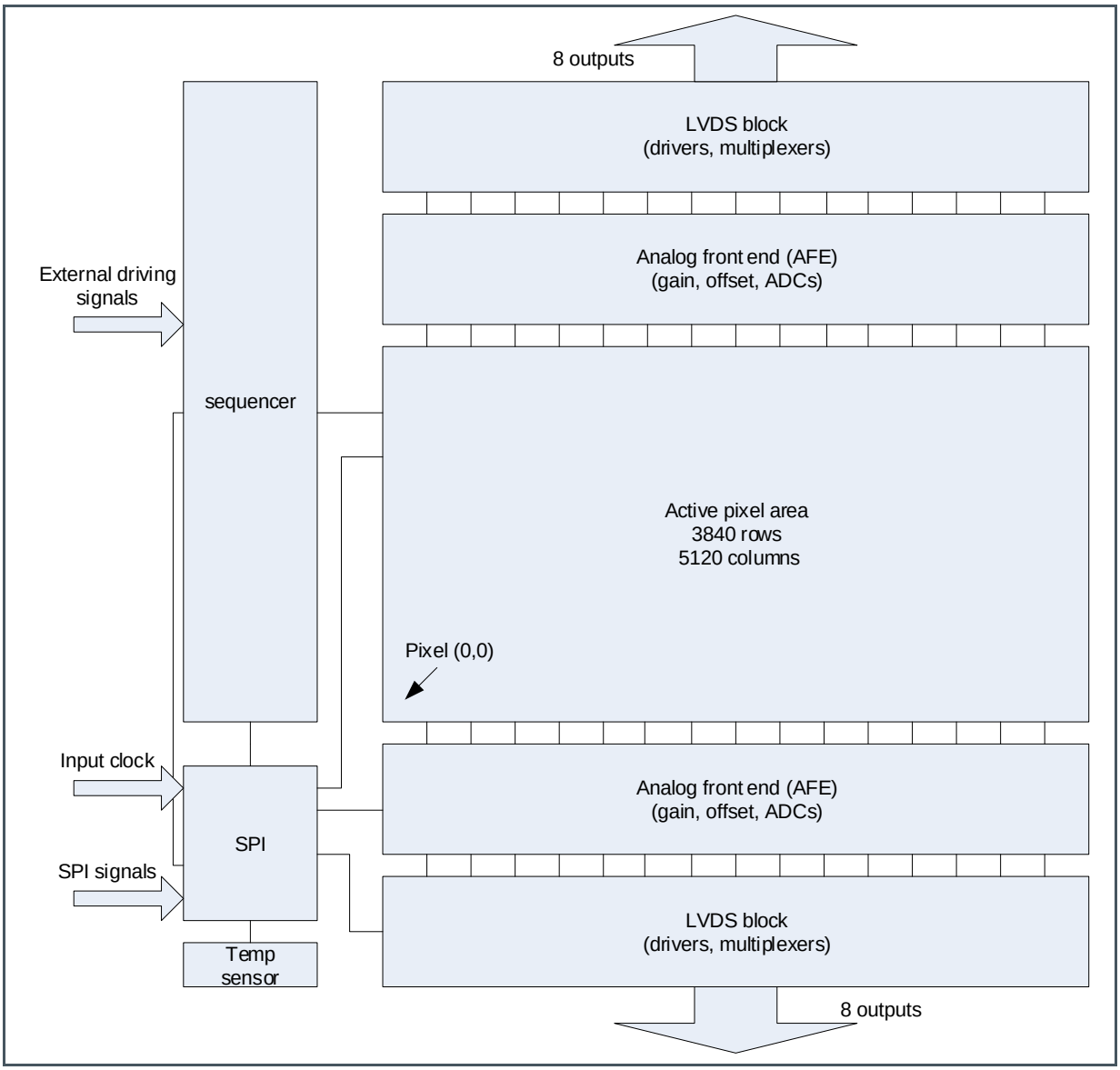
Attention

The CMV20000 is not allowed to be used in traffic applications.

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2 :
Functional Blocks of CMV20000



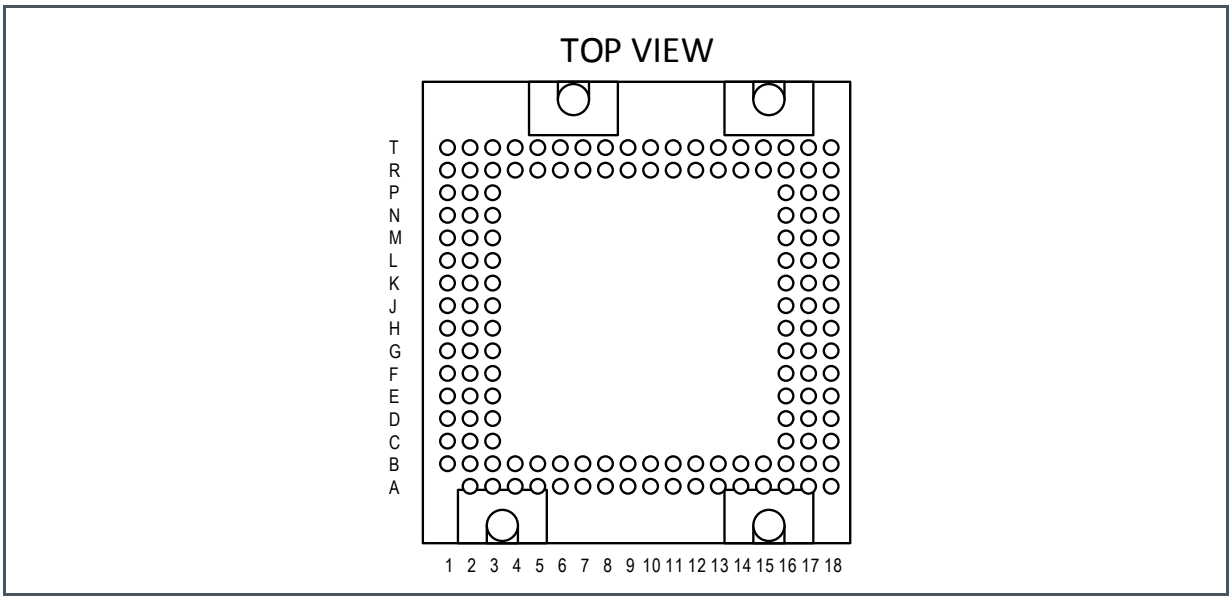
2 Ordering Information

Ordering Code	Package	Chroma	Options	Delivery Quantity
CMV20000-1E5M1PA	Ceramic PGA	Mono		10 pcs/tray
CMV20000-1E5C1PA	Ceramic PGA	Color		10 pcs/tray

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
Pin Diagram



3.2 Pin Description

Figure 4:
Pin Description of CMV20000

Pin	Pin Name	Pin Type	Description
A2	OUTE1_P	LVDS Output	LVDS positive output data even rows channel1 bottom
A3	VDD20	Supply	Digital blocks
A4	OUTE2_P	LVDS Output	LVDS positive output data even rows channel2 bottom
A5	VDD20	Supply	Digital blocks
A6	OUTE3_P	LVDS Output	LVDS positive output data even rows channel3 bottom
A7	VDDPIX	Supply	Pixel array power supply
A8	OUTE4_P	LVDS Output	LVDS positive output data even rows channel4 bottom
A9	GND	Ground	Ground pin
A10	OUTE5_N	LVDS Output	LVDS negative output data even rows channel5 bottom
A11	VDD20	Supply	Digital blocks

Pin	Pin Name	Pin Type	Description
A12	OUTE6_N	LVDS Output	LVDS negative output data even rows channel6 bottom
A13	VDDPIX	Supply	Pixel array power supply
A14	OUTE7_N	LVDS Output	LVDS negative output data even rows channel7 bottom
A15	GND	Ground	Ground pin
A16	OUTE8_N	LVDS Output	LVDS negative output data even rows channel8 bottom
A17	VDD20	Supply	Digital blocks
A18	CMD_LVDS	Bias	Decouple with 470 nF to ground
B1	DIO2	Test	Diode 2 for test (connect to GND)
B2	OUTE1_N	LVDS Output	LVDS negative output data even rows channel1 bottom
B3	GND	Ground	Ground pin
B4	OUTE2_N	LVDS Output	LVDS negative output data even rows channel2 bottom
B5	GND	Ground	Ground pin
B6	OUTE3_N	LVDS Output	LVDS negative output data even rows channel3 bottom
B7	GND	Ground	Ground pin
B8	OUTE4_N	LVDS Output	LVDS negative output data even rows channel4 bottom
B9	VDD33	Supply	Digital and analog
B10	OUTE5_P	LVDS Output	LVDS positive output data even rows channel5 bottom
B11	GND	Ground	Ground pin
B12	OUTE6_P	LVDS Output	LVDS positive output data even rows channel6 bottom
B13	GND	Ground	Ground pin
B14	OUTE7_P	LVDS Output	LVDS positive output data even rows channel7 bottom
B15	VDD33	Supply	Digital and analog
B16	OUTE8_P	LVDS Output	LVDS positive output data even rows channel8 bottom
B17	GND	Ground	Ground pin
B18	CMD_COL_AMPL	Bias	Decouple with 470 nF to ground
C1	TANA	Analog Output	Test pin for analog signals (can be left floating)
C2	OUTCTR_N	LVDS Output	LVDS negative control output channel
C3	DIO1	Test	Diode 1 for test (connect to GND)
C16	GND	Ground	Ground pin
C17	CMDN	Bias	Decouple with 470 nF to ground
C18	CMD_COL_PC	Bias	Decouple with 470 nF to ground
D1	TDIG2	Digital Output	Test pin for digital signals (can be left floating or route to an input pin of the FPGA)
D2	OUTCTR_P	LVDS Output	LVDS positive control output channel
D3	TDIG1	Digital Output	Test pin for digital signals (can be left floating or route to an input pin of the FPGA)
D16	CMDP	Bias	Decouple with 470 nF to VDD33
D17	CMDP_INV	Bias	Decouple with 470 nF to VDD33
D18	CMD_ADC	Bias	Decouple with 470 nF to VDD33
E1	Extra1		Leave floating
E2	Extra2		Connect to GND

Pin	Pin Name	Pin Type	Description
E3	FRAME_REQ	Digital Input	Frame request
E16	VBGAP	Bias	Decouple with 470 nF to VBGAP_LOW
E17	VBGAP_LOW	Bias	Decouple to VBGAP see pin E16
E18	CMD_COL_LOAD	Bias	Decouple with 470 nF to ground
F1	STRB_EXP1	Digital Output	Output strobe pin for the exposure time
F2	VDD20	Supply	Digital blocks
F3	GND	Ground	Ground pin
F16	GND	Ground	Ground pin
F17	VDD20	Supply	Digital blocks
F18	REF_ADC	Bias	Ref for ADC testing (decouple with 470 nF to ground)
G1	VDDPIX	Supply	Pixel array power supply
G2	GND	Ground	Ground pin
G3	VDD33	Supply	Digital and analog
G16	VDD33	Supply	Digital and analog
G17	GND	Ground	Ground pin
G18	VDDPIX	Supply	Pixel array power supply
H1	Extra6		Connect to GND
H2	T_EXP1	Digital Input	Input pin for external exposure mode
H3	GND	Ground	Ground pin
H16	GND	Ground	Ground pin
H17	VREF	Bias	Ref for column amps (decouple with 470 nF to ground)
H18	CMD_RAMP	Bias	Decouple with 470 nF to VDD33
J1	PLL_REF	Bias	Decouple with 470 nF to PLL_REF_LOW
J2	PLL_REF_LOW	Bias	Decouple to PLL_REF see pin J1
J3	GND	Ground	Ground pin
J16	GND	Ground	Ground pin
J17	VRAMP2	Bias	Start voltage second ramp (decouple with 470 nF to ground)
J18	VRAMP1	Bias	Start voltage first ramp (decouple with 470 nF to ground)
K1	VDDPIX	Supply	Pixel array power supply
K2	GND	Ground	Ground pin
K3	VDD33	Supply	Digital and analog
K16	VDD33	Supply	Digital and analog
K17	GND	Ground	Ground pin
K18	VDDPIX	Supply	Pixel array power supply
L1	LVDS_CLK_P	LVDS Input	LVDS input clock P
L2	VDD20	Supply	Digital blocks
L3	GND	Ground	Ground pin
L16	GND	Ground	Ground pin
L17	VDD20	Supply	Digital blocks
L18	SIG_ADC	Bias	Sig for ADC testing (decouple with 470 nF to ground)

Pin	Pin Name	Pin Type	Description
M1	LVDS_CLK_N	LVDS Input	LVDS input clock N
M2	CLK_IN	Digital Input	Master input clock
M3	SYS_RES_N	Digital Input	Input pin for sequencer reset
M16	VTF_LOW3	Bias	Transfer low voltage 3 (decouple with 470 nF to ground)
M17	VTF_LOW2	Bias	Transfer low voltage 2 (decouple with 470 nF to ground)
M18	VTF_LOW1	Bias	Transfer low voltage 1 (decouple with 470 nF to ground)
N1	Extra3		Connect to GND
N2	OUTCLK_P	LVDS Output	LVDS positive clock output channel
N3	Extra4		Connect to GND
N16	VRES_L	Bias	Res low voltage (decouple with 470 nF to ground)
N17	VRES_H	Supply	Pixel reset pulse
N18	VPCH_L	Bias	Precharge low voltage (decouple with 470 nF to ground)
P1	SPI_EN	Digital Input	SPI enable
P2	OUTCLK_N	LVDS Output	LVDS negative clock output channel
P3	SPI_IN	Digital Input	SPI data input pin
P16	GND	Ground	Ground pin
P17	GND	Ground	Ground pin
P18	VPCH_H	Bias	Precharge high voltage (decouple with 470 nF to ground)
R1	SPI_CLK	Digital Input	SPI clock input pin
R2	OUTO1_N	LVDS Output	LVDS negative output data odd rows channel1 top
R3	GND	Ground	Ground pin
R4	OUTO2_N	LVDS Output	LVDS negative output data odd rows channel2 top
R5	GND	Ground	Ground pin
R6	OUTO3_N	LVDS Output	LVDS negative output data odd rows channel3 top
R7	GND	Ground	Ground pin
R8	OUTO4_N	LVDS Output	LVDS negative output data odd rows channel4 top
R9	VDD33	Supply	Digital and analog
R10	OUTO5_P	LVDS Output	LVDS positive output data odd rows channel5 top
R11	GND	Ground	Ground pin
R12	OUTO6_P	LVDS Output	LVDS positive output data odd rows channel6 top
R13	GND	Ground	Ground pin
R14	OUTO7_P	LVDS Output	LVDS positive output data odd rows channel7 top
R15	VDD33	Supply	Digital and analog
R16	OUTO8_P	LVDS Output	LVDS positive output data odd rows channel8 top
R17	GND	Ground	Ground pin
R18	SPI_OUT_RIGHT	Digital Output	SPI data output pin at the right, this is a backup SPI data output pin. Only the SPI output data of register >= address 103 is available at this pin. Should be routed to the FPGA as well
T1	SPI_OUT_LEFT	Digital Output	SPI data output pin at the left, this is the main SPI data output pin containing the SPI output data of all registers.
T2	OUTO1_P	LVDS Output	LVDS positive output data odd rows channel1 top

Pin	Pin Name	Pin Type	Description
T3	VDD20	Supply	Digital blocks
T4	OUTO2_P	LVDS Output	LVDS positive output data odd rows channel2 top
T5	VDD20	Supply	Digital blocks
T6	OUTO3_P	LVDS Output	LVDS positive output data odd rows channel3 top
T7	VDDPIX	Supply	Pixel array power supply
T8	OUTO4_P	LVDS Output	LVDS positive output data odd rows channel4 top
T9	GND	Ground	Ground pin
T10	OUTO5_N	LVDS Output	LVDS negative output data odd rows channel5 top
T11	VDD20	Supply	Digital blocks
T12	OUTO6_N	LVDS Output	LVDS negative output data odd rows channel6 top
T13	VDDPIX	Supply	Pixel array power supply
T14	OUTO7_N	LVDS Output	LVDS negative output data odd rows channel7 top
T15	GND	Ground	Ground pin
T16	OUTO8_N	LVDS Output	LVDS negative output data odd rows channel8 top
T17	VDD20	Supply	Digital blocks
T18	Extra5		Connect to GND

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5
Absolute Maximum Ratings of CMV20000

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
VDD20	Digital blocks	1.7	2.2	V	
VDD33	Digital and analog	2.9	3.6	V	
VDDPIX	Pixel array power supply	2.6	3.6	V	
VRES_H	Pixel reset pulse	2.9	3.6	V	
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JEDEC JESD78D Nov 2011
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 2000		V	JS-001-2012
Temperature Ranges and Storage Conditions					
T_A	Operating Ambient Temperature	-20	70	°C	
T_{STRG}	Storage Temperature Range	- 20	50	°C	
RH_{NC}	Relative Humidity (non-condensing)		60	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor time of 168h

5 Electrical Characteristics

If not stated otherwise, all values are typical.

Figure 6:
Electrical Characteristics of CMV20000

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supplies						
VDD20	Digital blocks		2.0	2.1	2.2	V
VDD33	Digital and analog		3.2	3.3	3.4	V
VDDPIX	Pixel array power supply		2.9	3.0	3.1	V
VRES_H	Pixel reset pulse		3.2	3.3	3.4	V
IDD20	Supply current	Nominal Peak		800 1000		mA
IDD33	Supply current	Nominal Peak		170 600		mA
IDDPIX	Supply current	Nominal Peak		20 8000		mA
IRES_H	Supply current	Nominal Peak		5 100		mA
P_{tot}	Total Power Consumption			1100		mW
Digital I/O						
V_{IH}	High level input voltage		2.0		VDD33	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OH}	High level output voltage	VDD33 = 3.3 V I_{OH} = 2 mA	2.4			V
V_{OL}	Low level output voltage	VDD33 = 3.3 V I_{OL} = 2 mA			0.4	V
f_{CLK_IN}	CLK_IN frequency		10		40	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LVDS_CLK}	LVDS_CLK frequency		120		480	MHz
DC_{LVDS_CLK}	LVDS_CLK Duty cycle		45	50	55	%
f_{SPI_CLK}	SPI_CLK frequency				20	MHz
LVDS Receiver						
V_{ID}	Differential input voltage	Steady state	100	350	600	mV
V_{IC}	Receiver input range	Steady state	0.0		2.4	V
I_{ID}	Receiver input current	$V_{INP\|INN}$=1.2 V±50 mV, 0≤ $V_{INP\|INN}$≤2.4 V			20	µA
ΔI_{ID}	Receiver input current difference	$\|I_{INP} - I_{INN}\|$			6	µA
LVDS Driver						
V_{OD}	Differential output voltage	Steady State, R_L = 100 Ω	247	350	454	mV
ΔV_{OD}	Difference in V_{OD} between complementary output states	Steady State, R_L = 100 Ω			50	mV
V_{OC}	Common mode voltage	Steady State, R_L = 100 Ω	1.125	1.25	1.375	V
ΔV_{OC}	Difference in V_{OC} between complementary output states	Steady State, R_L = 100 Ω			50	mV
$I_{OS,GND}$	Output short circuit current to ground	V_{OUTP}=V_{OUTN}=GND			24	mA
$I_{OS,PN}$	Output short circuit current	V_{OUTP}=V_{OUTN}			12	mA

6 Typical Operating Characteristics

6.1 Electro-Optical Characteristics

Below are the typical electro-optical specifications of the CMV20000. These are the typical values for the whole operating range.

Figure 7:
Specification Overview

Parameter	Value	Remark
Effective pixels	5120 x 3840	
Pixel pitch	6.4 µm x 6.4 µm	
Optical size	32.77 mm x 24.58 mm	Full frame
Pixel type	Global shutter with true CDS	Allows fixed pattern noise correction and reset (kTC) noise cancelling by true correlated double sampling
Shutter type	Pipelined global shutter	Exposure of next image during readout of the previous image
Full well charge	15000 e-	Pinned photodiode pixel
Conversion gain	0.25 DN/e-	At recommended settings
Responsivity	0.29 A/W	@ 550 nm with micro lenses
Temporal noise	8 e-	Pipelined global shutter (GS) with correlated double sampling (CDS)
Dynamic range	66 dB	
SNR_{MAX}	41.8 dB	
PLS	1/50000	
DC	125 e-/s	At room temperature
FPN	< 0.2%	RMS of full swing
DSNU	10 e-/s	
PRNU	1%	RMS
Color filters	Optional	RGB Bayer
QE	64,5%	@ 550 nm with micro lenses
LVDS outputs	16	Each data output running at 480 Mbit/s. 8 outputs selectable at half frame rate.

Parameter	Value	Remark
Frame rate	30 fps	Using a 12bit/pixel and 480 Mbit/s LVDS. Higher frame rate possible in row windowing mode.
Timing generation	On-chip	Possibility to control exposure time through external pin.
PGA	Yes	4 analog gain settings
Programmable registers	Sensor parameters	Window coordinates, timing parameters, gain & offset, exposure time, flipped readout in X and Y direction.
HDR mode	Multi-slope	Multiple slopes with partial reset of the pixel.
ADC	12-bit	Column ADC
Interface	LVDS	Serial output data + synchronization signals
I/O Logic levels	LVDS = 2.1 V Logic levels = 3.3 V	
Cover glass	D263Teco	2 sides AR coating, no IR cut-off filter R < 2.2% abs, 400 nm – 900 nm, per surface, AOI = 15°

6.2 Spectral Characteristics

Figure 8:
Quantum Efficiency

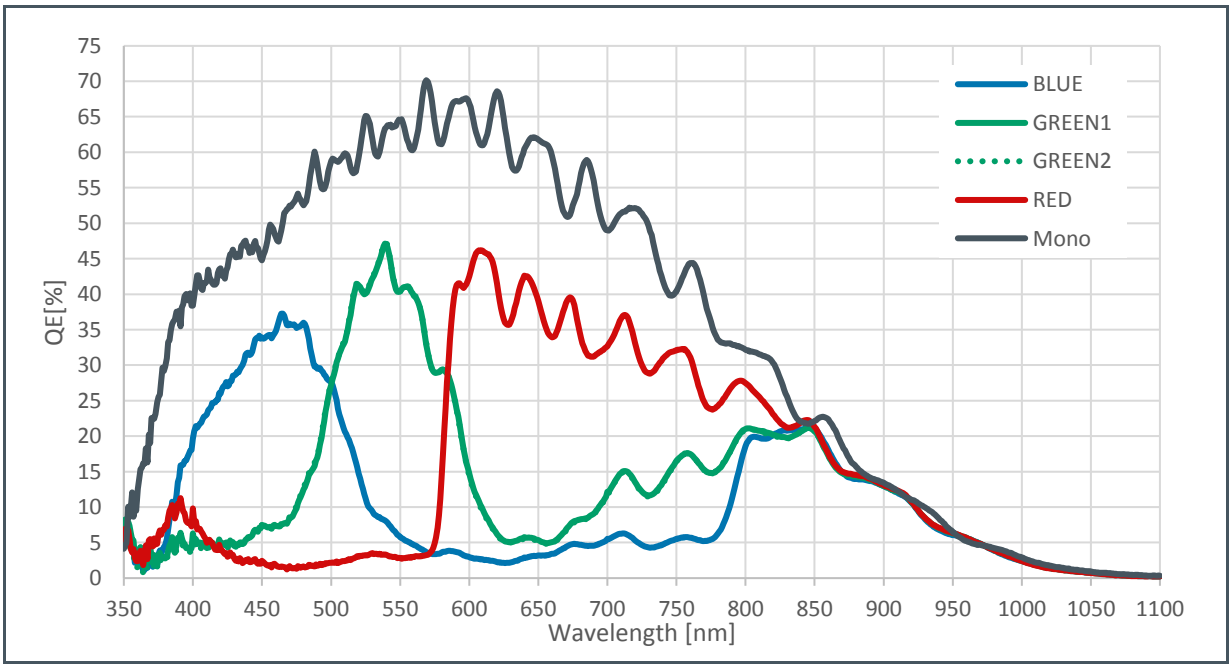


Figure 9:
Spectral Response

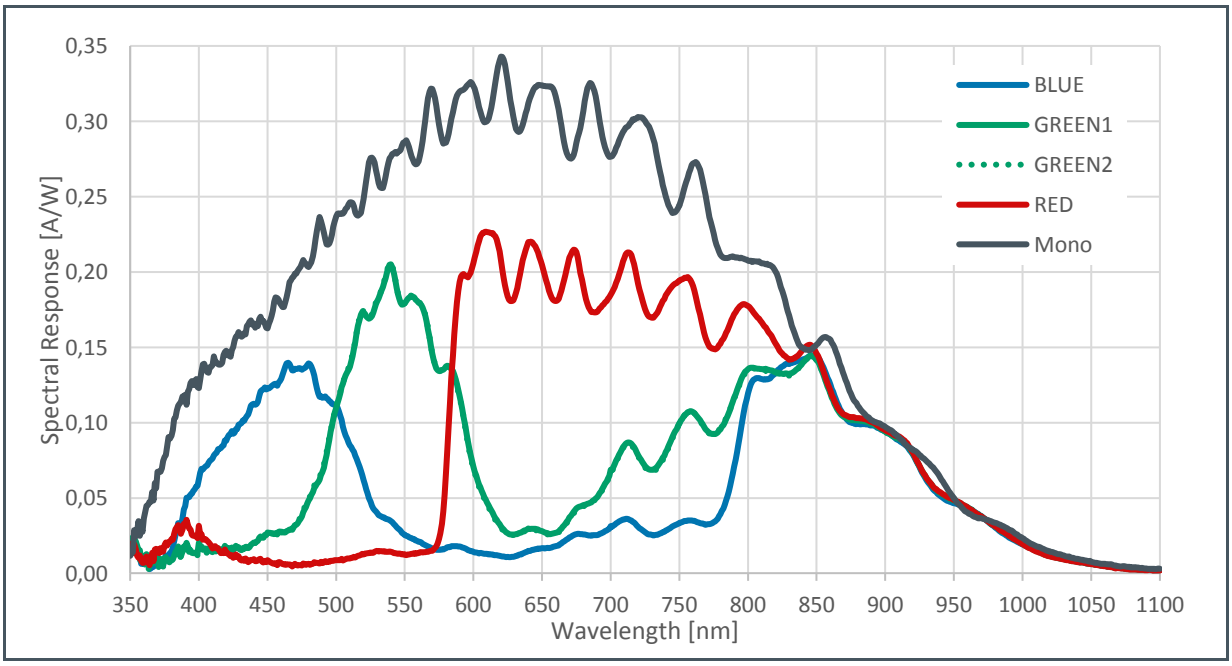
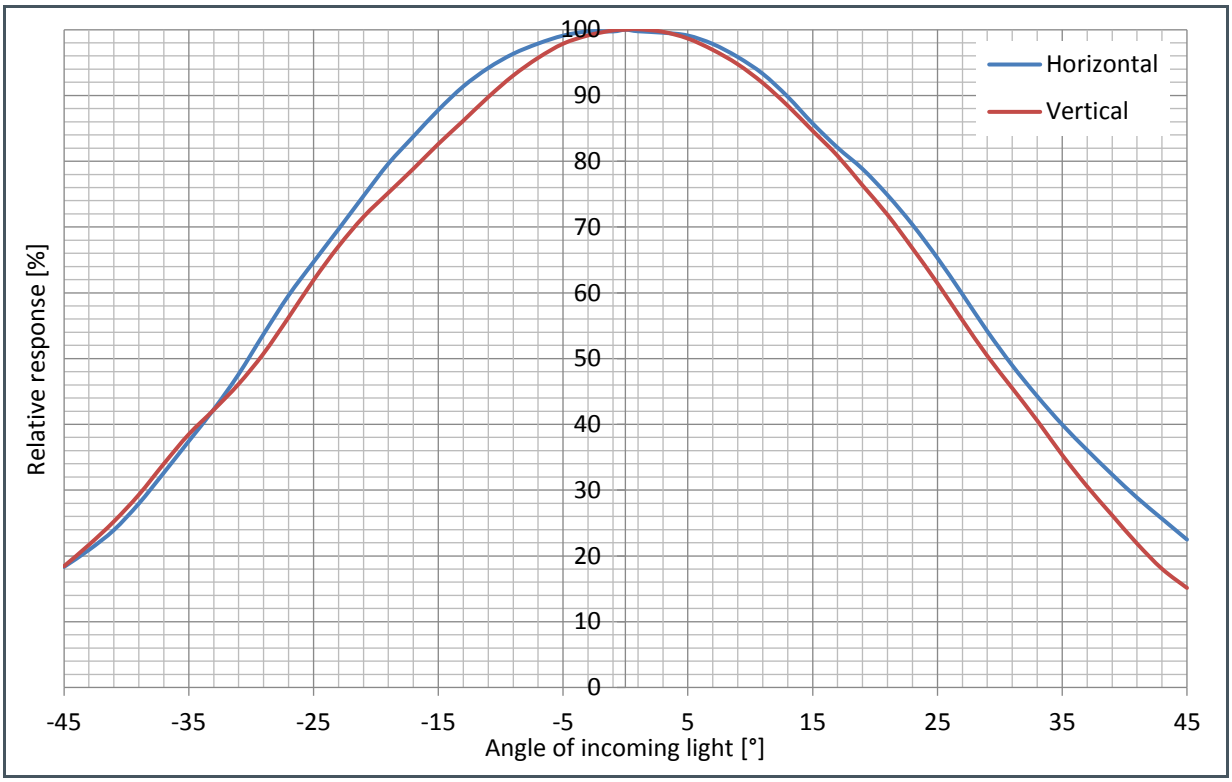


Figure 10:
Angular Response



7 Functional Description

7.1 Sensor Architecture

Figure 2 shows the image sensor architecture. The internal sequencer generates the necessary signals for image acquisition. The image is stored in the pixel (global shutter) and they are read out sequentially, row-by-row into the analog front-end electronics (AFE) of the columns. On the pixel output, an analog gain of x2.0, x2.4, x2.8 and x3.2 is possible (or 1.6, 1.9, 2.25, 2.55 when column calibration is on). The pixel value then passes to a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over multiple LVDS channels. Each LVDS channel reads out 640 adjacent columns of the array. The AFE and LVDS drivers are doubled on opposite sides of the sensor, resulting in 2 rows being read out at the same when all 16 outputs are used. In the Y-direction, rows of interest are selected through a row-decoder which allows a flexible windowing. Control registers are foreseen for the programming of the sensor. These register parameters are uploaded via a four-wire SPI interface. A temperature sensor which can be read out over the SPI interface is also included.

7.1.1 Pixel Array

The sensor has 5120 by 3840 active pixels with a 6.4 µm pitch surrounded by two dummy rows and columns. These dummy pixels at the side will ensure that the optical performance of the active pixels at the edge, is the same as the one in the active array. These dummy pixels cannot be read out and will be set permanently to the reset voltage. The pixels are designed to achieve maximum sensitivity with low noise and low PLS specification. Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency.

7.1.2 Analog Front-End Electronics (AFE)

The analog front-end consists of two major parts: a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies analog gain if desired (programmable using the SPI interface). The column ADC converts the analog pixel value to a 12-bit value and can adjust its ramp to compensate for small gain differences. All gain and offset settings can be programmed using the SPI interface.

7.1.3 LVDS Block

The LVDS block converts the digital data coming from the ADC into standard LVDS data running at maximum 480 Mbps. The sensor has 18 LVDS output pairs.

- 16 data channels
- 1 control channel
- 1 clock channel

The 16 data channels are used to transfer 12-bit data words from sensor to receiver. The output clock channel transports a DDR clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. The data on the control channel contains status information on the validity of the data on the data channels and other useful sensor status information.

7.1.4 Sequencer

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control clocks. This sequencer can be activated and programmed through the SPI interface.

7.1.5 SPI

The SPI interface is used to load the sequencer registers with data. The data in these registers is used by the sequencer while driving and reading out the image sensor. Features like windowing, sub sampling, gain and offset are programmed using this interface. The data in the on-chip registers can also be read back for test and debug of the surrounding system.

7.1.6 Temperature Sensor

A 16-bit digital temperature sensor is included in the image sensor and can be controlled by the SPI-interface. The on-chip temperature can be obtained by reading out a dedicated SPI register (address 101-102).

A calibration of the temperature sensor is needed by the surrounding system (for absolute temperature measurements).

7.2 Operating the Sensor

7.2.1 Power Supplies

External Power Supplies

The peak current of VDD20 is drawn during read out, while the other supplies draw it during FOT. All supplies should have enough decoupling, especially VDDPIX. Also VDD18 switches a lot of power per LVAL and should be equipped with a decent supply and decoupling. Noise on the VDD33 will be transferred to the image as row noise, so keep this supply as ‘clean’ as possible.

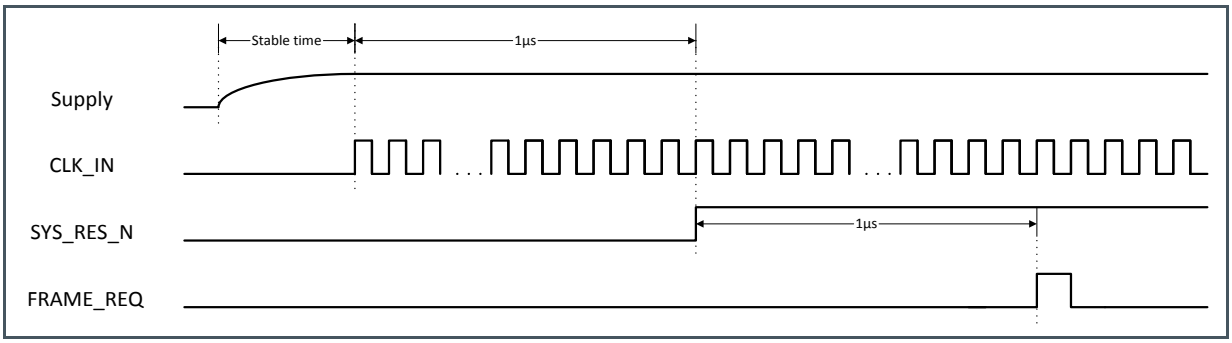
Biasing

For optimal performance, some pins need to be decoupled to ground or to VDD. Please refer to the pin list for a detailed description for every pin and the appropriate decoupling if applicable.

7.2.2 Startup Sequence

The following sequence should be followed when the device is started up in default output mode (480 Mbps, 12-bit resolution).

Figure 11:
Startup Sequence for 480 Mbps @12-bit

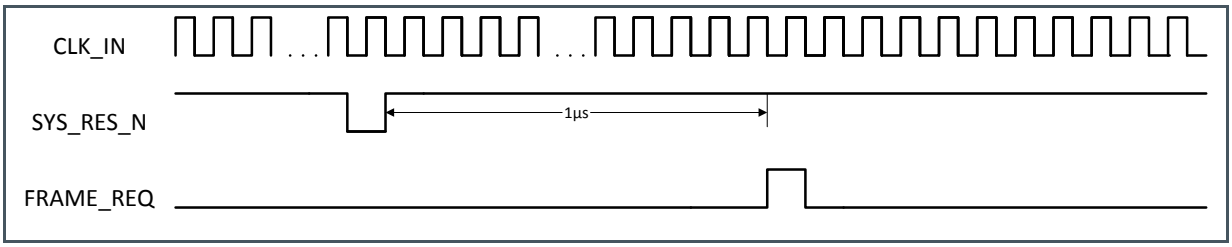


The CLK_IN and LVDS_CLK_N/P should only start after the rise time of the supplies (VDD33, VDD20, Vddpix and Vres_h go high together). The external reset pin should be released at least 1µs after the supplies have become stable. The first frame can be requested 1 µs after the reset pin has been released. An optional SPI upload (to program the sequencer) is possible 1 µs after the reset pin has been released. In this case the FRAME_REQ pulse must be postponed until after the SPI upload has been completed.

7.2.3 Reset Sequence

If a sensor reset is necessary while the sensor is running, the following sequence should be followed.

Figure 12:
Reset Sequence



The on-board sequencer will be reset and all programming registers will return to their default start-up values when a falling edge is detected on the SYS_RES_N pin. After the reset there is a minimum time of 1 µs needed before a FRAME_REQ pulse can be sent. All recommended register settings must be reloaded after a reset sequence.

7.2.4 SPI Programming

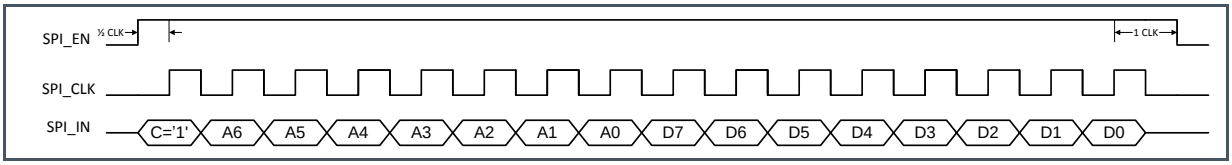
Programming the sensor is done by writing the appropriate values to the on-board registers. These registers can be written over a simple serial interface (SPI). The details of the timing and data format are described below. The data written to the programming registers can also be read out over this same SPI interface.

The SPI out does not have a tri-state, so multiple SPI outputs cannot be on the same bus without a buffer.

SPI Write

The timing to write data over the SPI interface can be found below.

Figure 13:
SPI Write



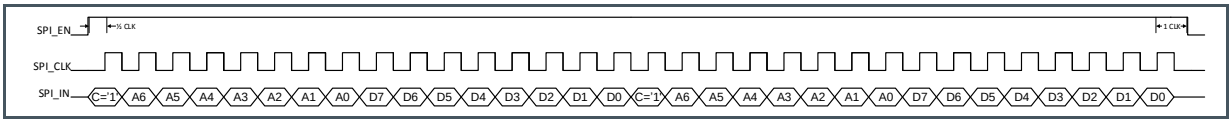
The data is sampled by the device on the rising edge of the SPI_CLK. The SPI_CLK has a maximum frequency of 20 MHz. The SPI_EN signal has to be high for half a clock period before the first data bit is sampled. SPI_EN has to remain high for 1 clock period after the last data bit is sampled.

One write action contains 16 data bits:

- One control bit: First bit to be sent, indicates whether a read (‘0’) or write (‘1’) will occur on the SPI interface.
- 7 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 8 data bits: These bits form the actual data that will be written in the register selected with the address bits. The data is written MSB first.

When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time. See the figure below for an example of 2 registers being written in burst.

Figure 14:
SPI Write of 2 Registers in Burst

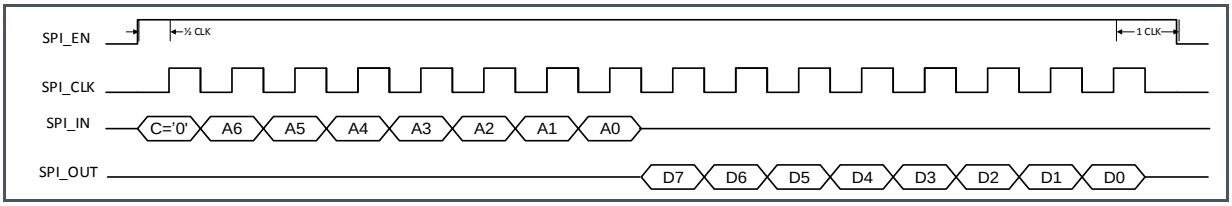


The sample and hold time is 1/4th of the SPI clock period.

SPI Read

The timing to read data from the registers over the SPI interface can be found below.

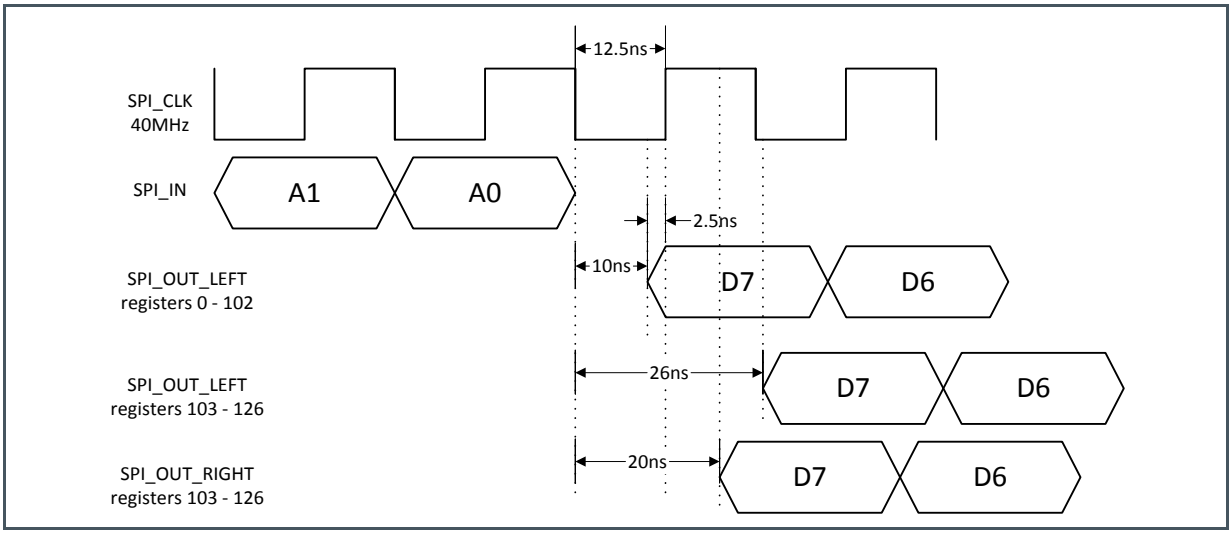
Figure 15:
SPI Read



To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is made '0'. The address of the register being read out is sent immediately after this control bit (MSB first). After the LSB of the address bits, the data is launched on the SPI_OUT pin on the falling edge of the SPI_CLK. This means that the data should be sampled by the receiving system on the rising edge of the SPI_CLK. The data comes over the SPI_OUT with MSB first.

The device has two SPI read out pins: SPI_OUT_LEFT (pin T1) and SPI_OUT_RIGHT (pin R18). SPI_OUT_LEFT will read out every register, while SPI_OUT_RIGHT will only read out registers 103 to 126. Because of the large sensor there is some SPI read out delay. This delay is fixed and independent of the sensor or SPI clock.

Figure 16:
SPI Delay



So when sampling on the rising SPI_CLK edge it is advised to have a SPI_CLK of 10 MHz maximum.

7.2.5 Requesting a Frame

After starting up the sensor (see section 7.2.2), a number of frames can be requested by sending a FRAME_REQ pulse. The number of frames can be set by programming the appropriate register (addresses 22 and 23). The default number of frames to be grabbed is 1.

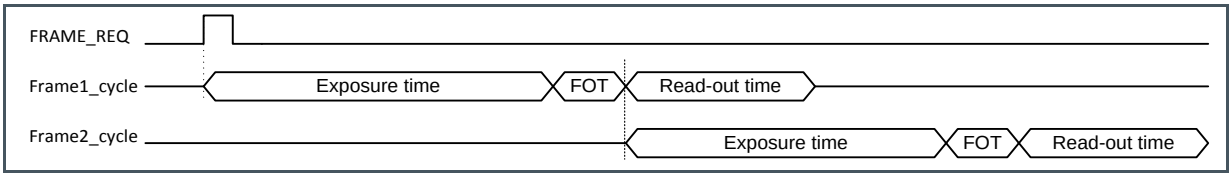
In internal exposure mode, the exposure time will start after this FRAME_REQ pulse. In the external exposure mode, the read-out will start after the FRAME_REQ pulse. Both modes are explained into detail in the sections below.

Internal Exposure Control

In this mode, the exposure time is set by programming the appropriate registers (address 32-33) of the device.

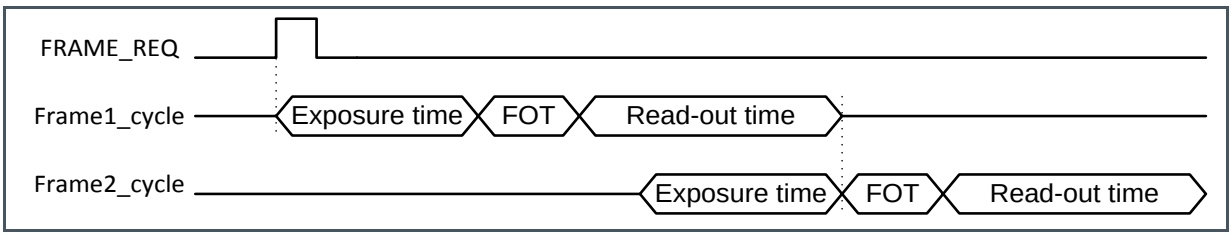
After the high state of the FRAME_REQ pulse is detected, the exposure time will start immediately. When the exposure time ends (as programmed in the registers), the pixels are being sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). Immediately after the FOT, the frame is read out automatically. If more than one frame is requested, the exposure of the next frame starts already during the read-out of the previous one. See the diagram below for more details.

Figure 17:
Internal Exposure Request for 2 Frames



When the exposure time is shorter than the read-out time, the FOT and read-out of the next frame will start immediately after the read-out of the previous frame.

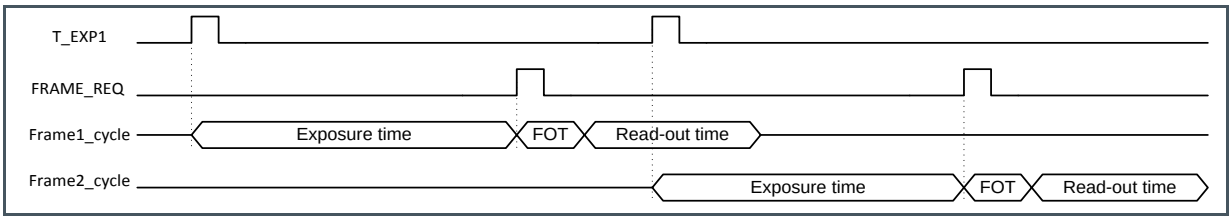
Figure 18:
Internal Exposure Request for 2 Frames with Exposure Time < Read-out Time



External Exposure Control

The exposure time can also be programmed externally by using the T_EXP1 input pin. This mode needs to be enabled by setting the appropriate register (address 81). In this case, the exposure starts when a high state is detected on the T_EXP1 pin. When a high state is detected on the FRAME_REQ input, the exposure time stops and the read-out will start automatically. A new exposure can start by sending a pulse to the T_EXP1 pin during or after the read-out of the previous frame.

Figure 19:
External Exposure Request for 2 Frames



7.3 Sensor Readout Format

7.3.1 LVDS Outputs

The device has LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Next to 16 data channels, the sensor also has two other LVDS channels for control and synchronization of the image data. In total, the sensor has 18 LVDS output pairs (2 pins for each LVDS channel):

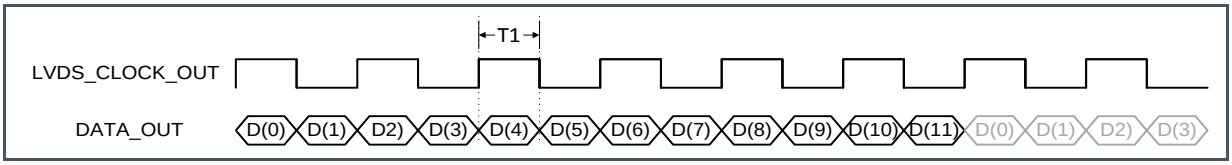
- 16 Data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 36 pins of the device are used for the LVDS outputs (32 for data + 2 for LVDS clock + 2 for control channel). See the pin list for the exact pin numbers of the LVDS outputs. The 16 data channels are used to transfer the 12-bit pixel data from the sensor to the receiver in the surrounding system. The output clock channel transports a clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. This clock is a DDR clock which means that the frequency will be half of the output data rate. When 480 Mbps output data rate is used, the LVDS output clock will be 240 MHz. The data on the control channel contains status information on the validity of the data on the data channels. Information on the control channel is grouped in 12-bit words that are transferred synchronous to the 16 data channels.

7.3.2 Low-Level Readout Format

The figure below shows the timing for transfer of 12-bit pixel data over one LVDS output. The figure shows only the p-channel of each LVDS pair. The data is transferred LSB first, with the transfer of bit D[0] during the high phase of the DDR output clock.

Figure 20:
12-bit Pixel Data on an LVDS Channel



The time T1 in the diagram above is 1/12th of the period of the input clock (CLK_IN) of the device. If a frequency of 40 MHz is used for CLK_IN (max), this results in a 240 MHz LVDS_CLOCK_OUT.

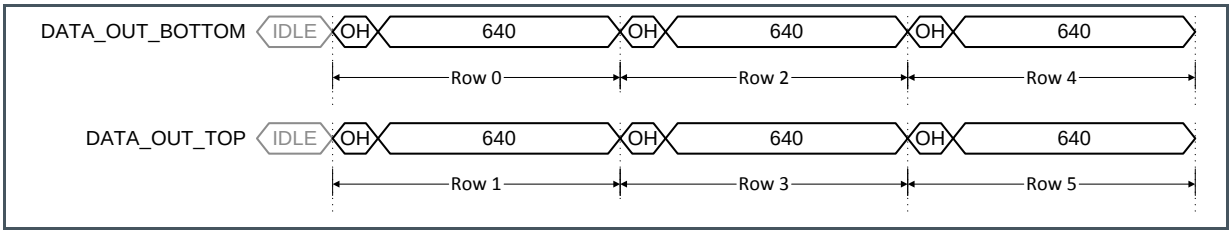
7.3.3 Pixel Readout Format

The readout of image data is grouped in bursts of 640 pixels per channel (2 rows at the same time). Each pixel is 12 bits of data. One complete pixel period equals one period of the master clock input. An overhead time exists between two bursts of 640 pixels. This overhead time has the length of one pixel read-out (i.e. the length of 12 bits at the selected data rate) or one master clock cycle.

16 Output Channels

By default, all 16 data output channels are used to transmit the image data. This means that two entire rows of image data are transferred in one slot of 640 pixel periods (16/2 x 640 = 5120). Figure 21 shows the timing for the top and bottom LVDS channels.

Figure 21:
Data Output Timing with 16 Channels

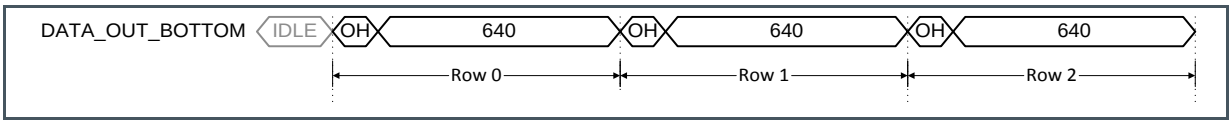


Only when 16 data outputs, running at 480 Mbps, are used, the frame rate of 30 fps can be achieved (default).

8 Output Channels

The device has the possibility to use only 8 LVDS output channels. This setting can be programmed in the register with address 80 (see section 7.5.1). In such multiplexed output mode, only the 8 bottom LVDS channels are used. The readout of one row takes 1*640 periods. This means that the entire rows of image data are transferred in one slot of 640 pixel periods (8 x 640 = 5120). Figure 22 shows the timing for the bottom LVDS channels.

Figure 22:
Data Output Timing With 8 Channels



In this 8 channel mode, the frame rate is reduced with a factor of 2 compared to 16 channel mode.

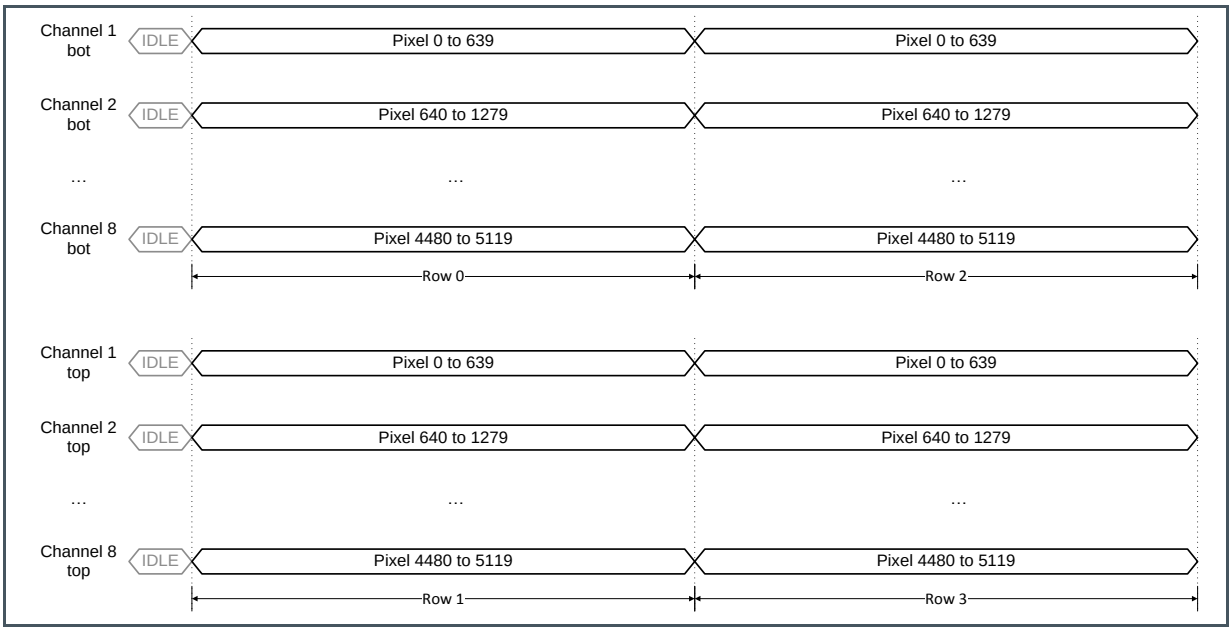
7.3.4 Pixel Remapping

Depending on the number of output channels, the pixels are read out by different channels and come out at a different moment in time. With the details from the next sections, the end user is able to remap the pixel values at the output to their correct image array location.

16 Outputs

The Figure 23 shows the location of the image pixels versus the output channel of the image sensor. 16 bursts (8 x 2) of 640 pixels happen in parallel on the data outputs. This means that two complete rows are read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default, there are 3840 rows being read out.

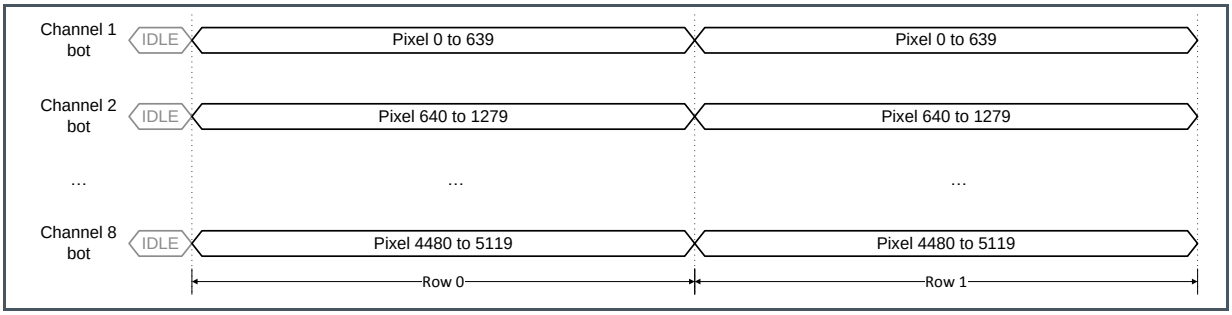
Figure 23:
Pixel Mapping Using 16 Output Channels



8 Outputs

When only 8 outputs are used, the pixel data is placed on the outputs as detailed in the figure below. 8 bursts of 640 pixels happen in parallel on the data outputs. This means that one complete row is read out in one burst. The time needed to read out two rows is doubled compared to when 16 outputs are used. The top LVDS channels are not being used in this mode, so they can be turned off by setting the correct bits in the register with address 95-97. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default, there are 3840 rows being read out.

Figure 24:
Pixel Mapping Using 8 Output Channels



7.3.5 Control Channel

The device has one LVDS output channel dedicated for the valid data synchronization and timing of the output channels. The end user must use this channel to know when valid image data or training data is available on the data output channels.

The control channel transfers status information in 12-bit word format. Every bit of the word has a specific function. Next figure describes the function of the individual bits.

Figure 25:
Control Channel Status Bits

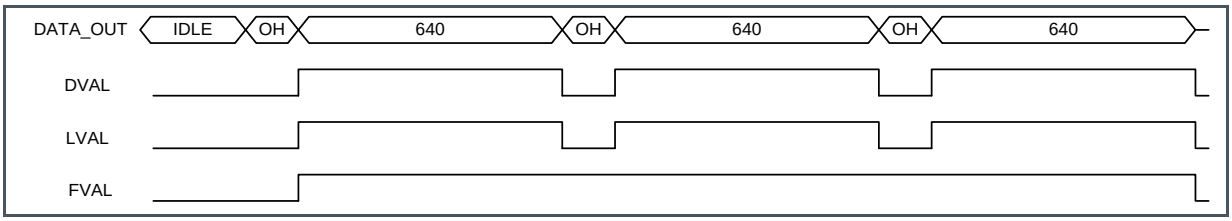
Bit	Function	Description
[0]	DVAL	Indicates valid pixel data on the outputs
[1]	LVAL	Indicates the validity of the read-out of a row
[2]	FVAL	Indicates the validity of the read-out of a frame
[3]	'0'	Constant zero
[4]	'0'	Constant zero
[5]	FOT	Indicates when the sensor is in FOT (sampling of image data in pixels)(1)
[6]	INTE1	Indicates when pixels of integration block 1 are integrating(1)
[7]	INTE2	Indicates when pixels of integration block 2 are integrating(1)
[8]	'0'	Constant zero
[9]	'1'	Constant one
[10]	'0'	Constant zero
[11]	'0'	Constant zero

(1) The status bits are purely informational. These bits are not required to know when the data is valid. The DVAL, LVAL and FVAL signals are sufficient to know when to sample the image data.

DVAL, LVAL, FVAL

The first three bits of the control word must be used to identify valid data and the readout status. Next figure shows the timing of the DVAL, LVAL and FVAL bits of the control channel with an example of the read-out of a frame of 6 rows (default is 3840 rows). This example uses the default mode of 16 outputs (8 outputs on each side).

Figure 26:
xVAL Timing in 16 Output Mode



Digital Test Pins

Pins D1 (Tdig2) and D3 (Tdig1) can be used as digital outputs to monitor the state of the sensor. Register 92 can be used to select a signal on these pins.

Figure 27:
Digital Test Pin D1

Reg98[6:4]	Tdig2
0	LVAL
3	INTE_1
7	CLK_out (=LVDS_CLK/12)

Figure 28:
Digital Test Pin D2

Reg92[3:0]	Tdig1
0	FVAL
2	FOT
3	INTE_2

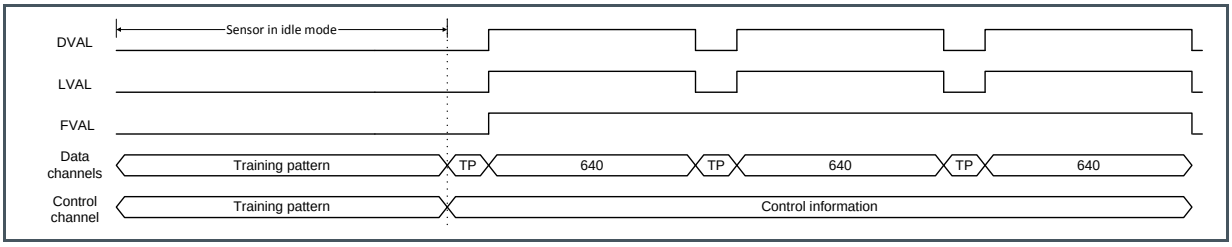
7.3.6 Training Data

To synchronize the receiving side with the LVDS outputs of the device, a known data pattern can be put on the output channels. This pattern can be used to “train” the LVDS receiver of the surrounding system to achieve correct word alignment of the image data. Such a training pattern is put on all 16 data channel outputs when there is no valid image data to be sent (so, also in between bursts of 640 pixels). The training pattern is a 12-bit data word that replaces the pixel data. The sensor has a 12-bit sequencer register (address 90-90) that can be loaded through the SPI to change the contents of the 12-bit training pattern.

The control channel does not send a training pattern, because it is used to send control information at all time. Word alignment can be done on this channel when the sensor is idle (not exposing or sending image data). In this case all bits of the control word are zero, except for bit [9].

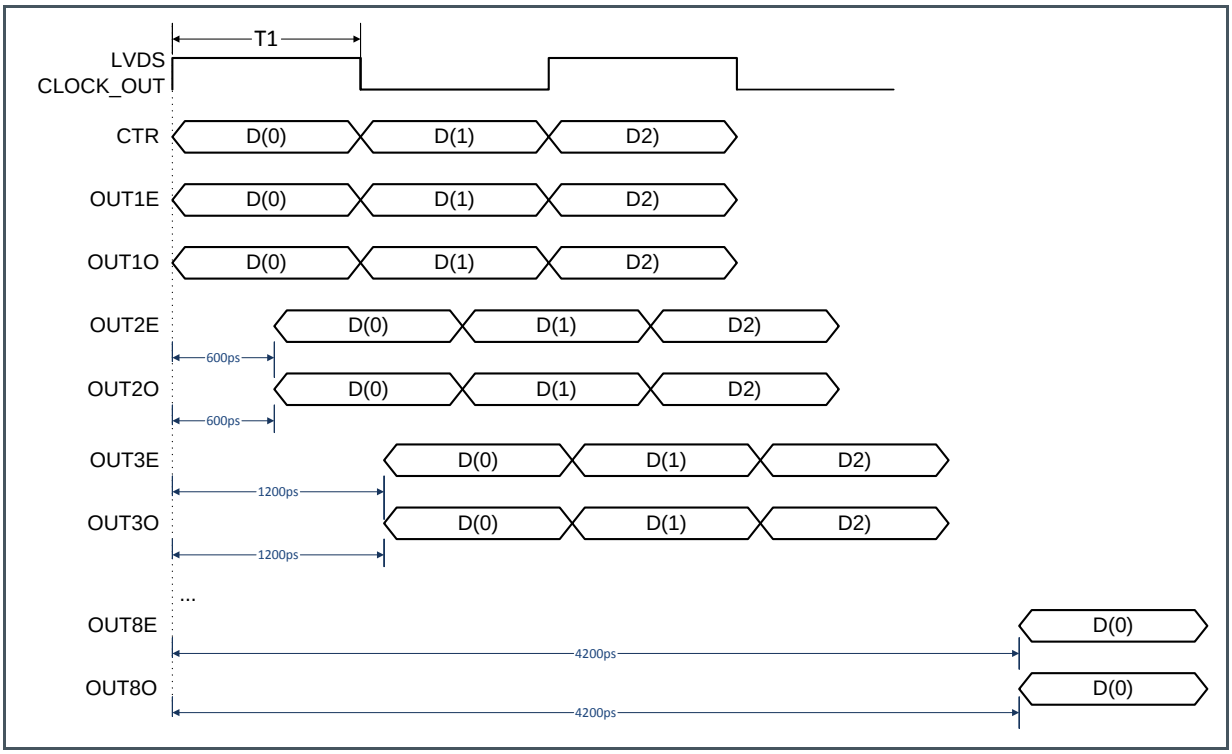
The figure below shows the location of the training pattern (TP) on the data channels and control channels when the sensor is in idle mode and when a frame of 6 rows is read out. The default mode of 16 outputs is selected.

Figure 29:
Training Pattern Timing



The LVDS outputs are not aligned with the LVDS output clock. Every channel (per odd/even side) has a skew of 600 ps compared to the previous channel. The control channel and both odd and even channels 1 are aligned with the clock. This skew will become larger than a LVDS clock period and therefore bit and word alignment is needed at the receiving side.

Figure 30:
LVDS Output Skew



7.3.7 Test Pattern

Instead of sending image data, the sensor can generate a fixed two-dimensional test image (after sending a frame request), if the test pattern mode is enabled. This setting can be programmed in the register by setting register 83[0] to 1.

The test pattern is the sum of the row number, the pixel number and the data output channel number. Figure 31 shows an example of the test pattern data.

Figure 31:
Test Pattern Data

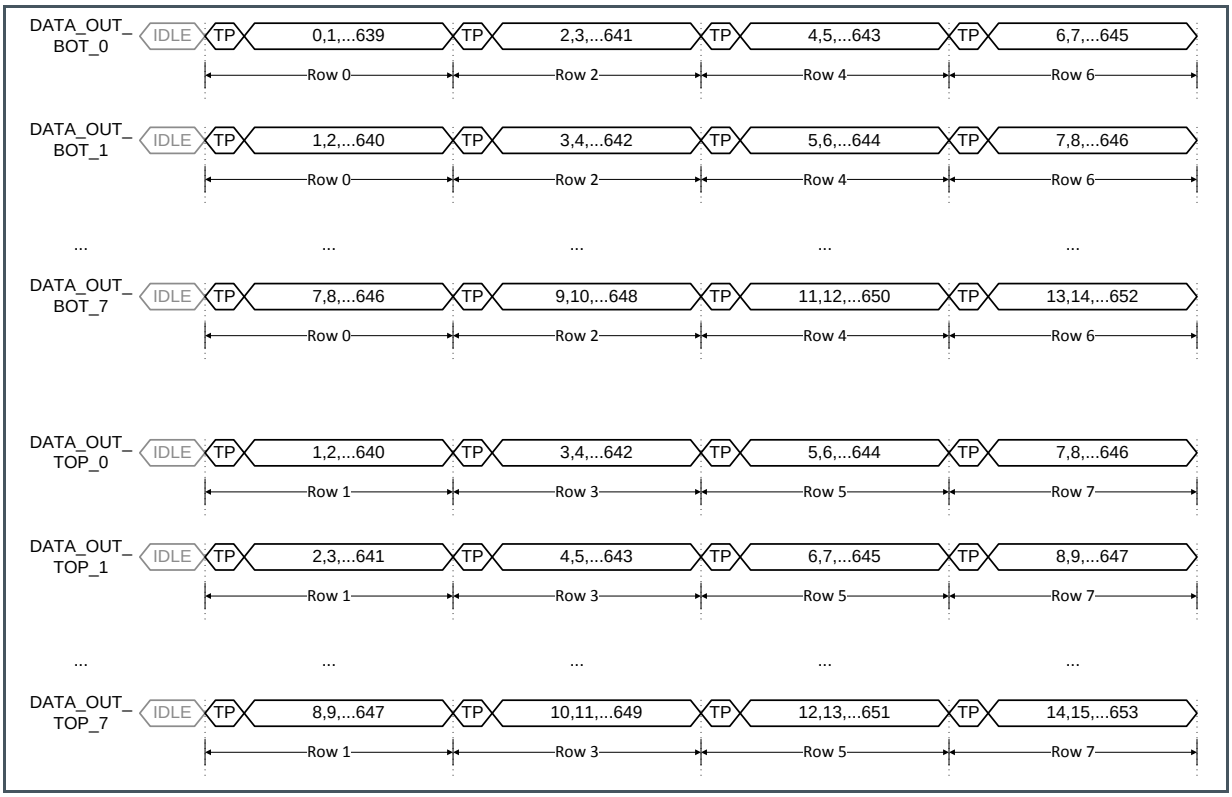
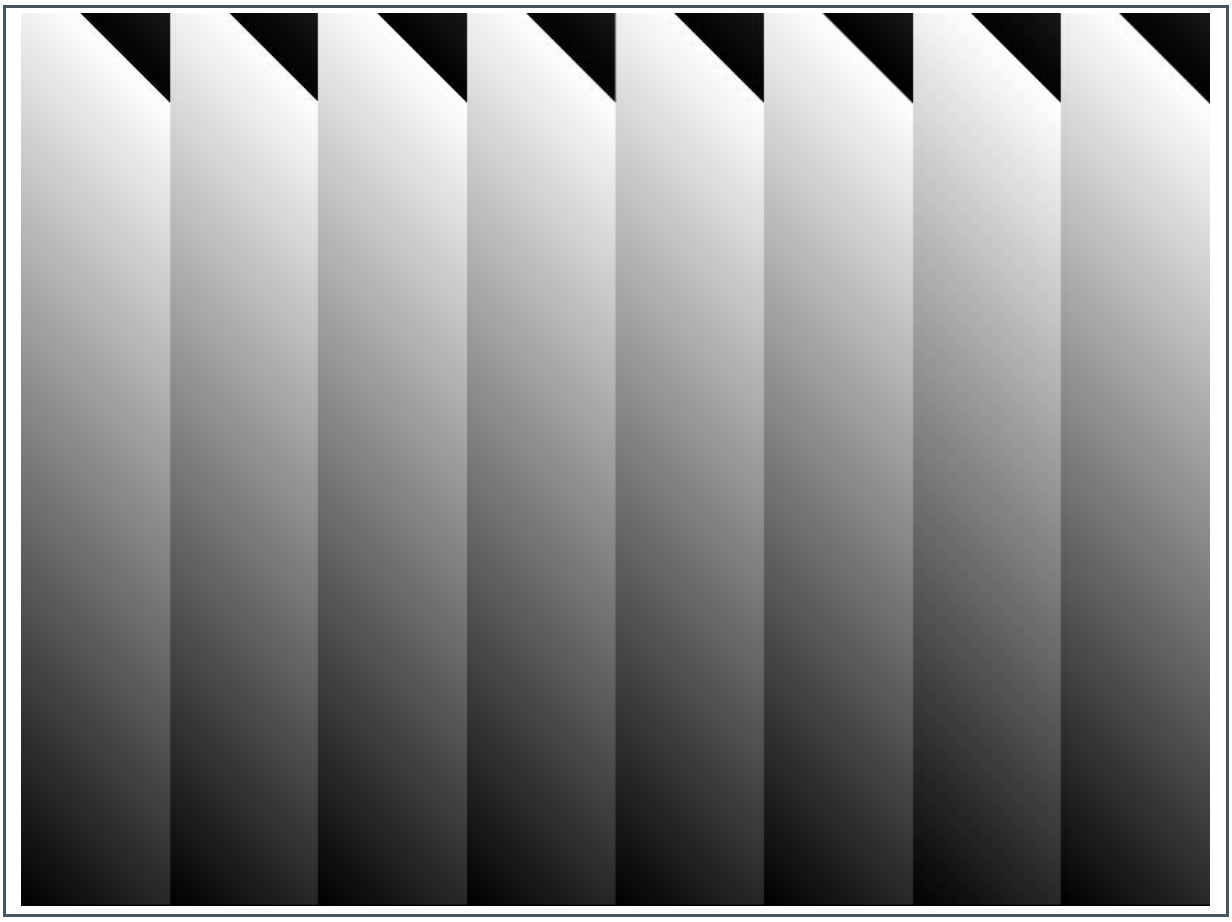


Figure 32:
Test Pattern Image



7.4 Configuring Readout and Exposure

This section explains how the CMV20000 can be programmed using the on-board sequencer registers

7.4.1 Exposure Modes

The exposure time can be programmed in two ways, externally or internally. Externally, the exposure time is defined as the time between the rising edge of T_EXP1 and the rising edge of FRAME_REQ (see section 7.2.5 for more details). Internally, the exposure time is set by uploading the desired value to the corresponding sequencer register.

Figure 33 gives an overview of the registers involved in the exposure mode.

Figure 33:
Exposure Modes

Reg. Name	Address	Default	Description
Exp_ext	81[0]	0	0: Exposure time is defined by the value uploaded in register 32-33. 1: Exposure time is defined by the pulses applied to the T_EXP1 and FRAME_REQ pins.
Exp_time	32-33	3840	When the Exp_ext register is set to '0', the value in this register defines the exposure time according to the formula below. Minimum =1

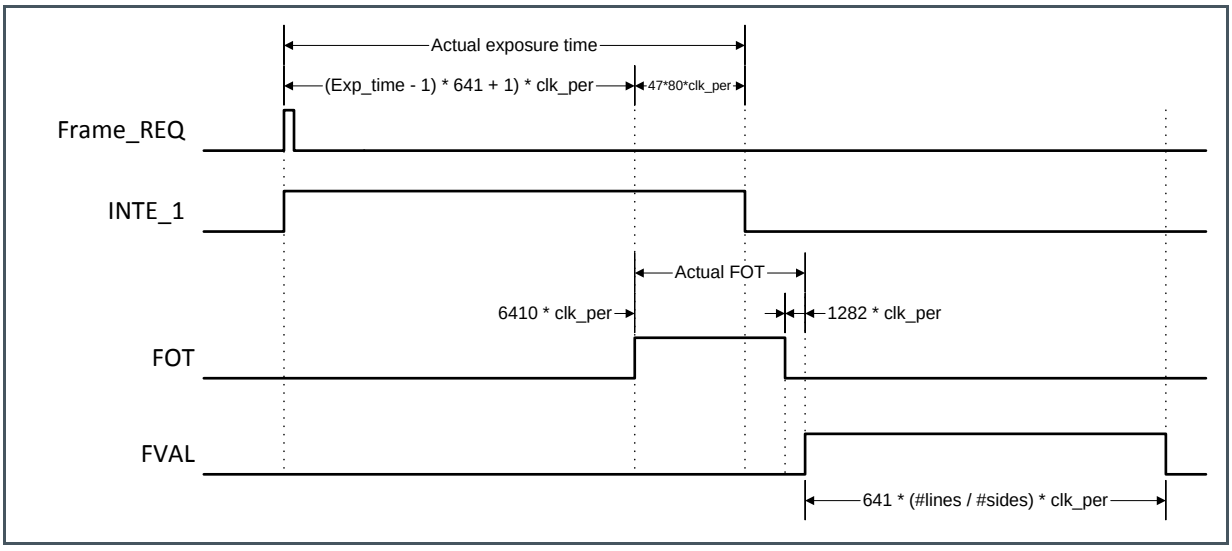
Equation 1:

$$Actual\ Exposure\ time = (((Exp"\_time" - 1) * 641) + 1 + (47 * reg82)) * clk\_per$$

Here clk_per is the period of the input LVDS_CLK multiplied by 12 (so for 480 MHz this is 25 ns). The minimum exposure time then becomes 94 µs.

A detailed view of the frame timing can be seen below.

Figure 34:
Frame Timing



7.4.2 Frame Timing

The frame rate of the CMV20000 is defined by 2 main factors.

- Exposure time
- Read out time

For ease of use we will assume that the exposure time is shorter than the read out time. By assuming this, the frame rate is completely defined by the read out time (because the exposure time happens in parallel with the read-out time). The read-out time (and thus the frame rate) is defined by:

- Output clock speed: max 480 Mbps
- Number of lines read-out
- Number of outputs used: max 16 LVDS outputs (8 on the top and 8 on the bottom)

This means that if any of the parameters above are changed, it will have an impact on the frame rate of the sensor. In normal operation (16 outputs @ 480 Mbps, 12-bit and full resolution) this will result in 30 fps.

The total readout time is composed of two parts:

- FOT (frame overhead time)
- Image readout time

The FOT is defined as

Equation 2:

$$FOT = \left(\left(80 * reg82 + \frac{reg82}{8}\right) + (2 * 641)\right) * clk\_per$$

So for reg82 = 80 and running at 480 MHz this becomes:

Equation 3:

$$FOT = (6410 + 1282) * 25ns = 192.3\mu s$$

The image read out time equals to

Equation 4:

$$Read\ Out\ Time = 641 * clk\_per * \frac{nr\_lines}{\#\ sides\ used}$$

So for full resolution and running at 480 MHz with both output sides used this becomes:

Equation 5:

$$Read\ Out\ Time = 641 * 25ns * \frac{3840}{2} = 30.768ms$$

This results in a total frame time of:

Equation 6:

$$Frame\ time = FOT + Read\ Out\ time$$

So for the default settings this becomes:

Equation 7:

$$Frame\ time = 192.3\mu s + 30768\ \mu s = 30.96ms$$

And the frame rate becomes:

Equation 8:

$$Frame\ rate = \frac{1}{Frame\ time} = \frac{1}{0.03096s} = 32.3fps$$

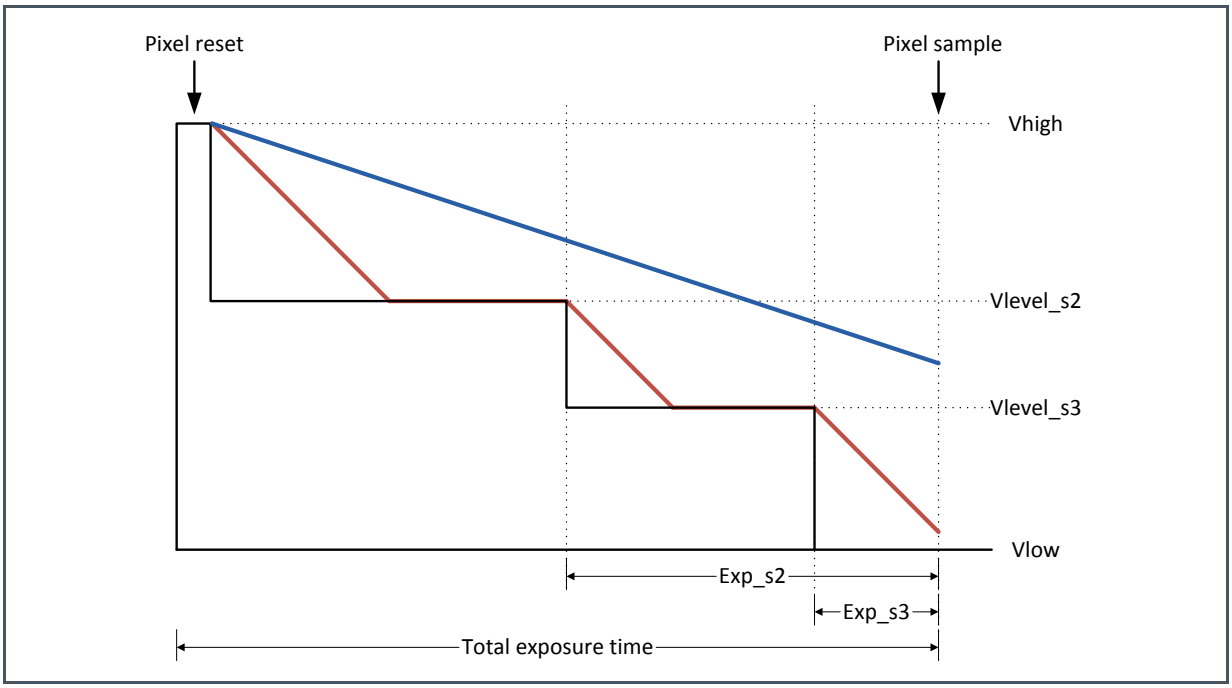
See section 7.4.1 for detailed frame timing. Clk_per is the period of the pixel clock. This pixel clock frequency is equal to 1/12th (40 MHz) of the LVDS input clock frequency (480 MHz).

7.4.3 High Dynamic Range Modes

Piecewise Linear Response

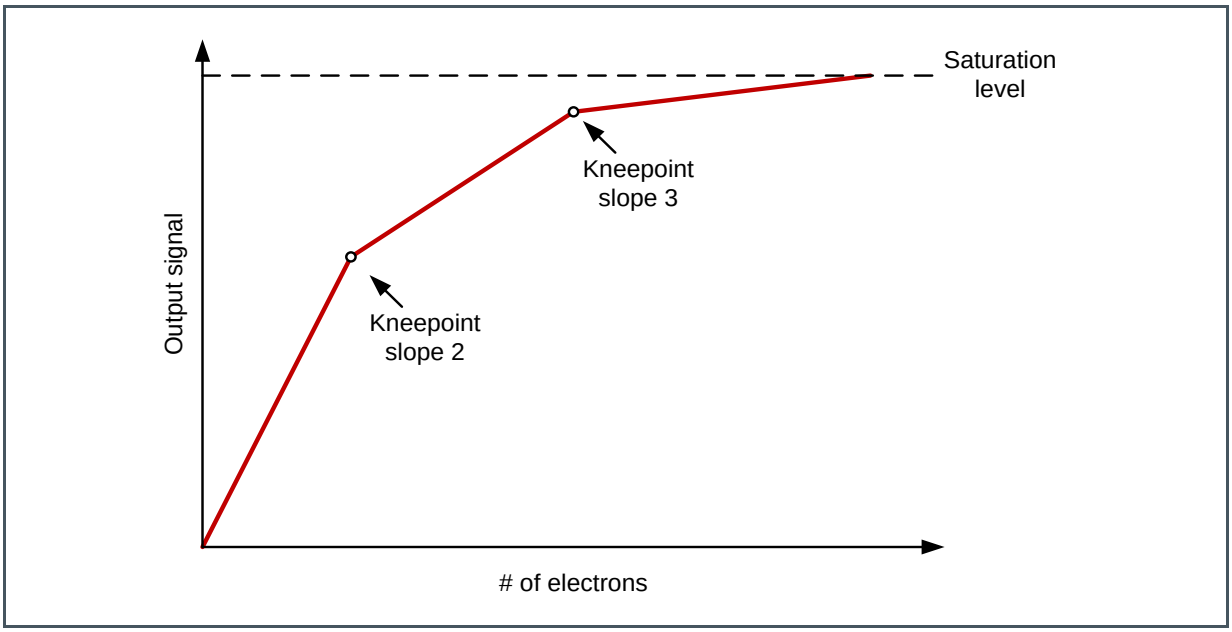
The device has the possibility to achieve a high optical dynamic range by using a piecewise linear response. This feature will clip illuminated pixels which reach a programmable voltage, while leaving the darker pixels untouched. The clipping level can be adjusted 2 times within one exposure time to achieve a maximum of 3 slopes in the response curve. More details can be found in the Figure 35.

Figure 35:
Piecewise Linear Response Details



In the figure above, the red lines represent a pixel on which a large amount of light is falling. The blue line represents a pixel on which less light is falling. As shown in the figure, the bright pixel is held to a programmable voltage for a programmable time during the exposure time. This happens two times to make sure that at the end of the exposure time the pixel is not saturated. The darker pixel is not influenced and will have a normal response. The Vlevel_s2/3 voltages and different exposure times are programmable using the sequencer registers. Using this feature, a response as detailed in Figure 36 can be achieved. The placement of the kneepoints in X is controlled by the Vlevel_s2/3 programming, while the slope of the segments is controlled by the programmed exposure times.

Figure 36:
Piecewise Linear Response



Piecewise Linear Response with Internal Exposure Mode

The following registers need to be programmed when a piecewise linear response in internal exposure mode is desired.

Figure 37:
HDR Settings - PLR

Reg. Name	Address	Default	Description
Exp_time	32-33	3840	The value in this register defines the total exposure time according following formula: ((Exp_time - 1) x 641 + 1 + 47 x FOT_mult) x clk_per, where clk_per is the period of the master input clock.
Nr_slopes	37[1:0]	1	The value in this register defines the number of slopes (min=1, max=3).
Exp_s2	39-40	0	The value in this register defines the exposure time from the start of the second slope to the end of the total exposure time. Formula: ((Exp_s2 - 1) x 641 + 1 + 47 x FOT_mult) x clk_per, where clk_per is the period of the master input clock.

Reg. Name	Address	Default	Description
Exp_s3	42-43	0	The value in this register defines the exposure time from the start of the third slope to the end of the total exposure time. Formula: ((Exp_s3 - 1) x 641 + 1 + 47 x FOT_mult) x clk_per, where clk_per is the period of the master input clock.
Vlevel_s2	114[6:0]	64	Bit [6] = Enable Bit [5:0] = DAC value Low level voltage during dual slope operation. The value in this register defines the Vlevel_s2 voltage (DAC setting). The DAC range goes from 0 to 2.1 V.
Vlevel_s3	115[6:0]	64	Bit [6] = Enable Bit [5:0] DAC value Low level voltage during triple slope operation. The value in this register defines the Vlevel_s3 voltage (DAC setting). The DAC range goes from 0 to 2.1 V.

Piecewise Linear Response with External Exposure Mode

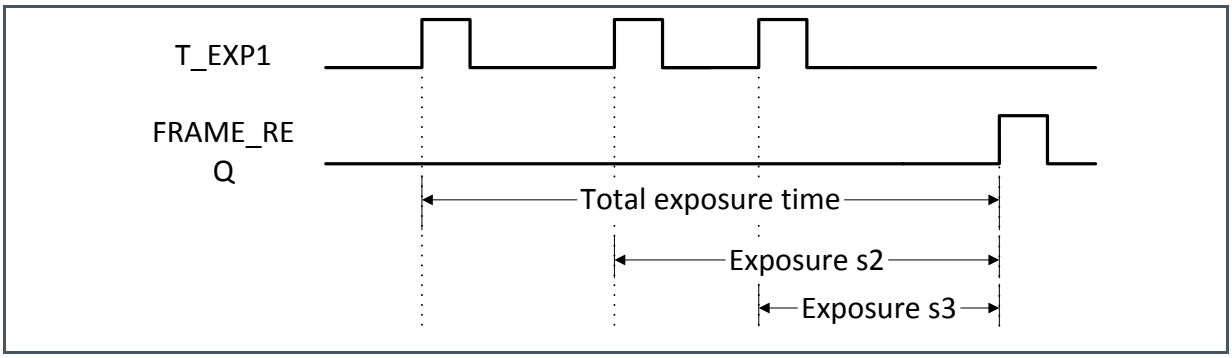
When external exposure time is used and a piecewise linear response is desired, the following registers should be programmed,

Figure 38:
HDR Settings - PLR

Reg. Name	Address	Default	Description
Nr_slopes_ex	15[1:0]	1	The value in this register defines the number of slopes (min=1, max=3).
Vlevel_s2_ex	112[6:0]	64	Bit [6] = Enable Bit [5:0] = DAC value Low level voltage during dual slope operation. The value in this register defines the Vlevel_s2 voltage (DAC setting). The DAC range goes from 0 to 2.1 V.
Vlevel_s3_ex	113[6:0]	64	Bit [6] = Enable Bit [5:0] = DAC value Low level voltage during triple slope operation. The value in this register defines the Vlevel_s3 voltage (DAC setting). The DAC range goes from 0 to 2.1 V.

The timing that needs to be applied in this external exposure mode looks like the one in Figure 39.

Figure 39:
PLR With External Exposure Mode



7.4.4 Windowing

To limit the amount of data or to increase the frame rate of the sensor, windowing in Y direction is possible. The number of lines and start address can be set by programming the appropriate registers. The CMV20000 has the possibility to read out multiple (max=8) predefined sub-windows in one read-out cycle. The default mode is to read-out one window with the full frame size (5120 x 3840).

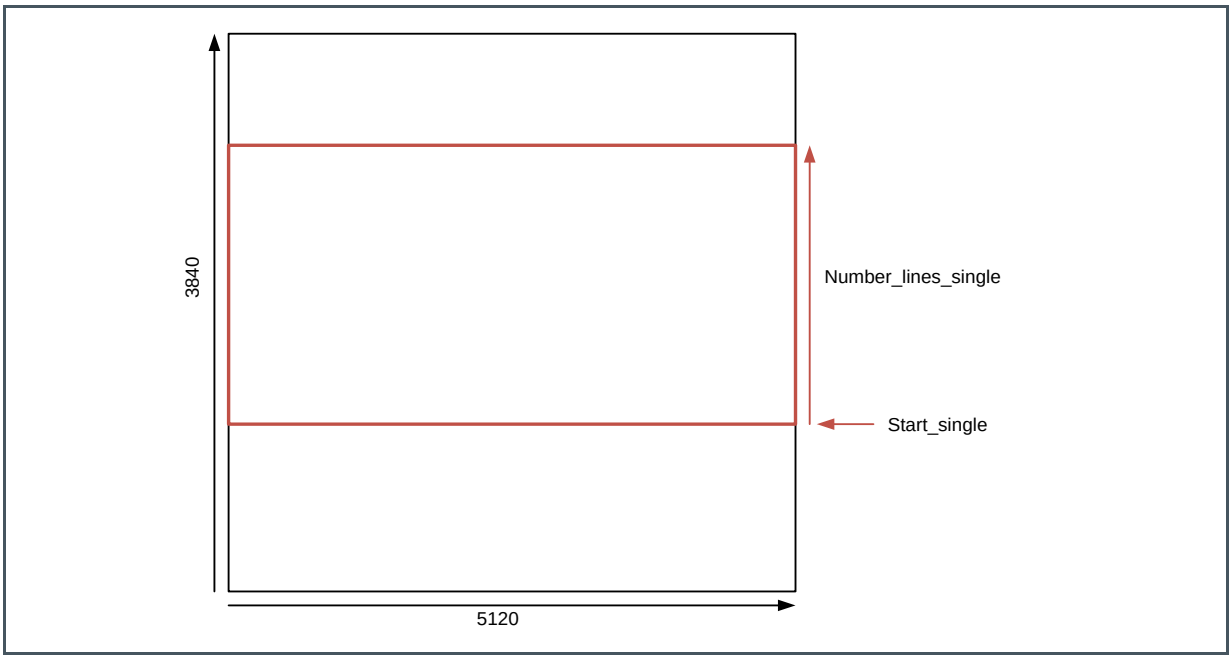
Single Window

When a single window is read out, the start address and size can be uploaded in the corresponding registers. The default start address is 0 and the default size is 3840 (full frame).

Figure 40:
Single Window Settings

Reg. Name	Address	Default	Description
Start_single	24-25	0	The value in this register defines the start address of the window in Y (min=0, max=3839)
Number_lines_single	26-27	3840	The value in this register defines the number of lines read out by the sensor (min=1, max=3840)

Figure 41:
Single Window



Multiple Windows

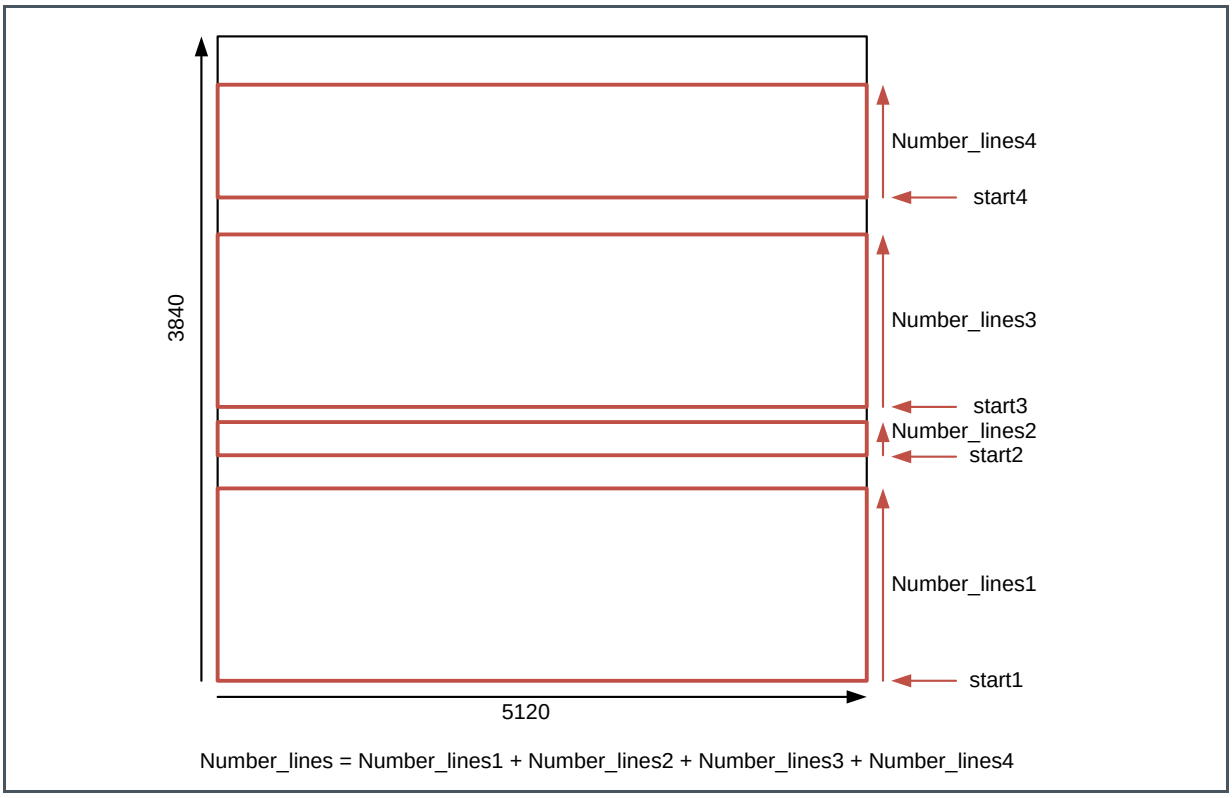
The CMV20000 can read out a maximum of 8 different sub-windows in one read-out cycle. The location and length of these sub-windows must be programmed in the correct registers. The total number of lines to be read-out (sum of all windows) needs to be specified in the Number_lines register. The registers which need to be programmed for the multiple windows can be found in the table below.

Figure 42:
Multiple Window Settings

Reg. Name	Address	Default	Description
Multwin_en	44	0	0: Multiple windows mode disabled 1: Multiple windows mode enabled
Number_lines	45-46	0	The value in this register defines the total number of lines read-out by the sensor (min=1, max=3840)
Start1	47-48	0	The value in this register defines the start address of the first window in Y (min=0, max=3839)
Number_lines1	63-64	0	The value in this register defines the number of lines of the first window (min=1, max=3840)
Start2	49-50	0	The value in this register defines the start address of the second window in Y (min=0, max=3839)
Number_lines2	65-66	0	The value in this register defines the number of lines of the second window (min=1, max=3840)

Reg. Name	Address	Default	Description
Start3	51-52	0	The value in this register defines the start address of the third window in Y (min=0, max=3839)
Number_lines3	67-68	0	The value in this register defines the number of lines of the third window (min=1, max=3840)
Start4	53-54	0	The value in this register defines the start address of the fourth window in Y (min=0, max=3839)
Number_lines4	69-70	0	The value in this register defines the number of lines of the fourth window (min=1, max=3840)
Start5	55-56	0	The value in this register defines the start address of the fifth window in Y (min=0, max=3839)
Number_lines5	71-72	0	The value in this register defines the number of lines of the fifth window (min=1, max=3840)
Start6	57-58	0	The value in this register defines the start address of the sixth window in Y (min=0, max=3839)
Number_lines6	73-74	0	The value in this register defines the number of lines of the sixth window (min=1, max=3840)
Start7	59-60	0	The value in this register defines the start address of the seventh window in Y (min=0, max=3839)
Number_lines7	75-76	0	The value in this register defines the number of lines of the seventh window (min=1, max=3840)
Start8	61-62	0	The value in this register defines the start address of the eighth window in Y (min=0, max=3839)
Number_lines8	77-78	0	The value in this register defines the number of lines of the seventh window (min=1, max=3840)

Figure 43:
Example of 4 Sub-Windows Read-Out



7.4.5 Image Flipping

The image coming out of the image sensor, can be flipped in X and/or Y direction. This means that if flipping is enabled in both directions the upper right pixel is read out first (instead of lower left). The following registers are involved in image flipping.

Figure 44:
Image Flipping

Reg. Name	Address	Default	Description
Image_flipping	85[1:0]	0	0: No image flipping 1: Image flipping in X 2: Image flipping in Y 3: Image flipping in X and Y

7.4.6 Image Subsampling

To maintain the same field of view but reduce the amount of data coming out of the sensor, a subsampling mode is implemented on the chip. Different subsampling schemes can be programmed by setting the appropriate registers. These subsampling schemes can take into account whether a color or monochrome sensor is used to preserve the Bayer pattern information. The registers involved in subsampling are detailed below. A distinction is made between a simple and advanced mode (can be used for color devices). Subsampling can be enabled in every windowing mode.

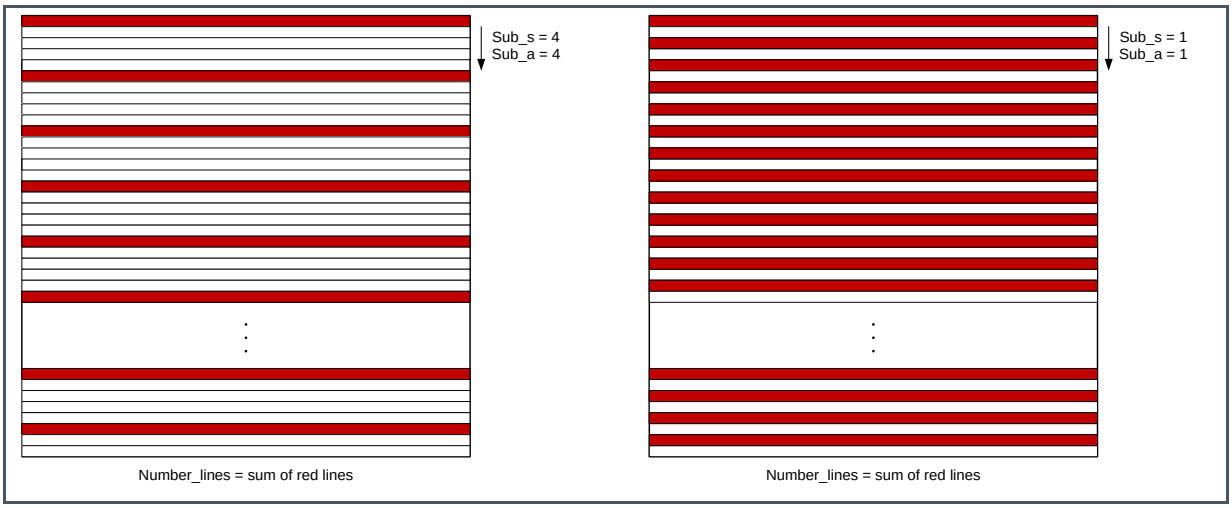
Simple Subsampling

Figure 45:
Simple Subsampling

Reg. Name	Address	Default	Description
Number_lines_single	26-27	3840	The value in this register defines the total number of lines read out by the sensor (min=1, max=3840)
Sub_s	28-29	0	Number of rows to skip (min=0, max=3839)
Sub_a	30-31	0	Identical to Sub_s

The figures below give two subsampling examples (skip 4x and skip 1x).

Figure 46:
Subsampling Examples in Simple Mode (Left: Skip 4x and Right: Skip 1x)



Advanced Subsampling

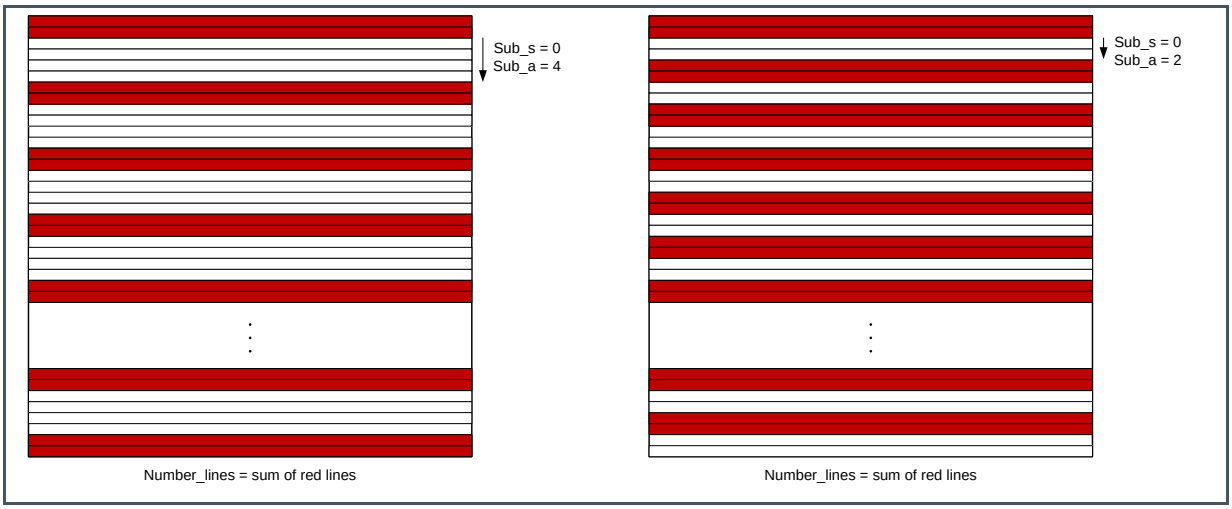
When a color sensor is used, the subsampling scheme should take into account that a Bayer color filter is applied on the sensor. This Bayer pattern should be preserved when subsampling is used. This means that the number of rows to be skipped should always be a multiple of two. An advanced subsampling scheme can be programmed to achieve these requirements. Of course, this advanced subsampling scheme can also be programmed in a monochrome sensor. See the table of registers in Figure 47 for more details.

Figure 47:
Advanced Subsampling

Reg. Name	Address	Default	Description
Number_lines_single	26-27	3840	The value in this register defines the total number of lines read out by the sensor (min=1, max=3840)
Sub_s	28-29	0	Should be '0' at all times
Sub_a	30-31	0	Number of rows to skip, it should be an even number between 0 and 3839

Figure 48 shows two subsampling examples (skip 4x and skip 2x) in advanced mode.

Figure 48:
Subsampling Examples in Advanced Mode (Left: Skip 4x and Right: Skip 2x)



7.4.7 Number of Frames

When internal exposure mode is selected, the number of frames sent by the sensor after a frame request can be programmed in the corresponding sequencer register.

Figure 49:
Number of Frames

Reg. Name	Address	Default	Description
Number_frames	22-23	1	The value in this register defines the number of frames grabbed and sent by the image sensor in internal exposure mode (min =1, max = 65535)

7.4.8 FOT Multiplier

The length of the FOT can be programmed using the register below. It is not recommended to set it below 80 as loss in swing and increase in FPN can occur.

Figure 50:
FOT Multiplier

Reg. Name	Address	Default	Description
FOT_mult	82	80	The value in this register defines the length of the FOT according to the following formula: (80 x FOT_mult + FOT_mult/8) x clk_per, where clk_per is the period of the master input clock (min=8, max=248, multiple of 8)

7.5 Configuring Output Data Format

7.5.1 Output Mode

When LVDS output mode is selected, the number of LVDS channels can be selected by programming the appropriate sequencer register. The pixel remapping scheme and the read-out timing for each mode can be found in section 7.3 of this document.

Figure 51:
Output Mode

Reg. Name	Address	Default	Description
Output_mode	80	0	0: 16 outputs 1: 8 outputs

7.5.2 Training Pattern

As detailed in section 7.3.6, a training pattern is sent over the LVDS data channels whenever no valid image data is sent. This training pattern can be programmed using the sequencer register.

Figure 52:
Training Pattern

Reg. Name	Address	Default	Description
Training_pattern	90-91	85	The 12LSBs of this 16-bit word are sent

7.5.3 Test Pattern

As detailed in section 7.3.7, a test pattern can be generated whenever no training data is sent. This test pattern can be enabled using the register below.

Figure 53:
Test Pattern

Reg. Name	Address	Default	Description
Testpattern_en	83	0	0: Test pattern disabled 1: Test pattern enabled

7.5.4 Data Rate

During start-up or after a sequencer reset, the data rate can be changed if a lower speed than 480 Mbps is desired. This can be done by applying a lower master input clock (CLK_IN) and lower LVDS_CLK_N/P to the sensor. See section 5 for more details on the input clock. See section 7.2.2 and 7.2.3 for details on how and when the data rate can be changed.

7.5.5 Power Control

The power consumption of the device can be regulated by disabling the LVDS data channels when they are not used (in 8 channel mode).

Figure 54:
Power Control

Reg. Name	Address	Default	Description
Channel_en	95-96	262143	Bits 0-7 : Enable/disable the bottom data output channels Bits 8-15 : Enable/disable the top data output channels Bit 16 : Enables/disables the clock channel Bit 17 : Enables/disables the control channel Bit 18 : Enables/disables the clock receiver 0: Disabled 1: Enabled

7.6 Configuring On-Chip Data Processing

7.6.1 Offset

A digital offset can be applied to the output signal. The dark level offset can be programmed by setting the desired value in the sequencer registers. The offset register is a 12-bit 2's complement representation of the actual desired offset to be added or subtracted from a fixed value of 1296. The default offset register value of 2840 is the 2's complement representation of -1256. Hence, the default dark level is 1296 + (-1256) = 40.

Figure 55:
Offset

Reg. Name	Address	Default	Description
Offset	88-89	2840	The value in this register defines the dark level offset applied to the output signal

7.6.2 Gain

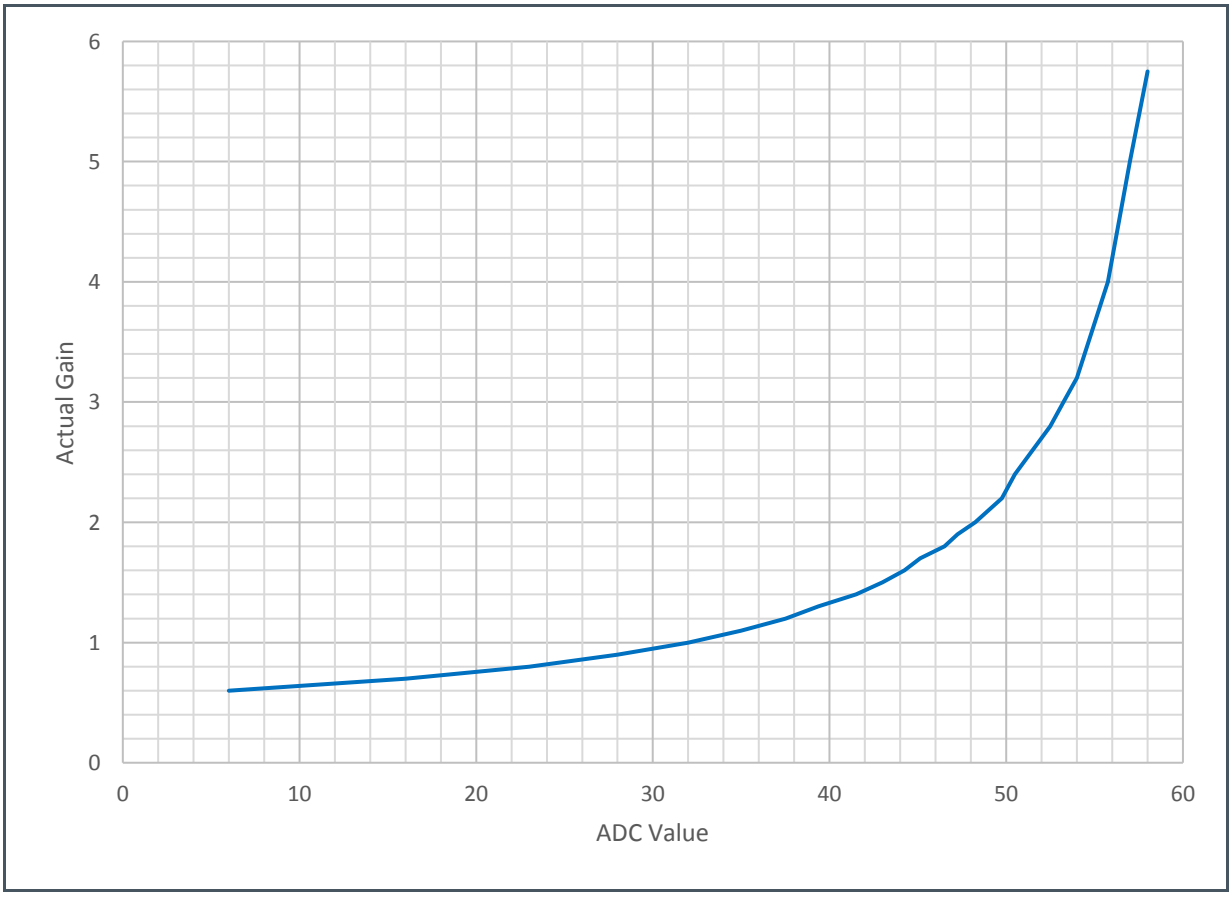
An analog gain and ADC gain can be applied to the output signal. The analog gain is applied by a PGA in every column. The digital gain is applied by the ADC. The ADC gain has to be changed when changing the clock speed from 480 MHz.

Figure 56:
Gain

Reg. Name	Address	Default	Description
PGA_gain	93 bits[3:2]	0	0: x0.8 1: x1 (recommended) 2: x1.2 4: x1.4
ADC_gain	126 bits[5:0]	32	32

The figure below illustrates the ADC_gain setting vs. the actual gain. When for example you run the sensor at 240 MHz, you have to use an actual gain of 480/240 = x2 or value 48 to compensate (the ADC conversion is dependent on the clock speed).

Figure 57:
ADC Gain Versus Actual Gain



7.7 Additional Features

7.7.1 Temperature

The register below contains the temperature data.

Figure 58:
Temperature

Reg. Name	Address	Default	Description
Temperature	101-102	0	This register contains the temperature data

8 Register Description

8.1 Register Overview

The table below gives an overview of all the sensor registers. The registers with the remark “Do not change” should not be overwritten.

Figure 59:
Register Overview

Address	Register Name(s)	Default Value	Fixed Value[1]
0		1	Do not change
1		0	Do not change
2		0	Do not change
3		0	Do not change
4		0	Do not change
5		15	Do not change
6		0	Do not change
7		0	Do not change
8		0	Do not change
9		0	Do not change
10		32	Do not change
11		0	Do not change
12		32	Do not change
13		0	Do not change
14		0	Do not change
15	Nr_slopes_ex[1:0]	1	
16		0	Do not change
17		0	Do not change
18		0	Do not change
19		0	Do not change
20		0	Do not change
21		0	Do not change
22	Number_frames[7:0]	1	
23	Number_frames[15:8]	0	
24	Start_single[7:0]	0	
25	Start_single[15:8]	0	
26	Number_lines_single[7:0]	0	
27	Number_lines_single[15:8]	15	
28	Sub_s[7:0]	0	

Address	Register Name(s)	Default Value	Fixed Value(1)
29	Sub_s[15:8]	0	
30	Sub_a[7:0]	0	
31	Sub_a[15:8]	0	
32	Exp_time[7:0]	0	
33	Exp_time[15:8]	15	
34		0	Do not change
35		15	Do not change
36		0	Do not change
37	Nr_slopes[1:0]	1	
38		0	Do not change
39	Exp_s2[7:0]	0	
40	Exp_s2[15:8]	0	
41		0	Do not change
42	Exp_s3[7:0]	0	
43	Exp_s3[15:8]	0	
44	Multwin_en	0	
45	Number_lines[7:0]	0	
46	Number_lines[15:8]	0	
47	Start1[7:0]	0	
48	Start1[15:8]	0	
49	Start2[7:0]	0	
50	Start2[15:8]	0	
51	Start3[7:0]	0	
52	Start3[15:8]	0	
53	Start4[7:0]	0	
54	Start4[15:8]	0	
55	Start5[7:0]	0	
56	Start5[15:8]	0	
57	Start6[7:0]	0	
58	Start6[15:8]	0	
59	Start7[7:0]	0	
60	Start7[15:8]	0	
61	Start8[7:0]	0	
62	Start8[15:8]	0	
63	Number_lines1[7:0]	0	
64	Number_lines1[15:8]	0	
65	Number_lines2[7:0]	0	
67	Number_lines2[15:8]	0	
68	Number_lines3[7:0]	0	
69	Number_lines3[15:8]	0	

Address	Register Name(s)	Default Value	Fixed Value[1]
70	Number_lines4[7:0]	0	
71	Number_lines4[15:8]	0	
72	Number_lines5[7:0]	0	
73	Number_lines5[15:8]	0	
74	Number_lines6[7:0]	0	
75	Number_lines6[15:8]	0	
76	Number_lines7[7:0]	0	
77	Number_lines7[15:8]	0	
78	Number_lines8[7:0]	0	
79		0	Do not change
80	Output_mode	0	
81	Exp_ext	0	
82	FOT_mult[7:0]	80	
83	Testpattern_en	0	
84		129	131
85	Image_flipping[1:0]	0	
86		0	3
87		254	0
88	Offset[7:0]	24	
89	Offset[11:8]	11	
90	Training_pattern[7:0]	85	
91	Training_pattern[15:8]	0	
92		0	Do not change
93	PGA_Gain[3:2]	0	
94		136	72
95	Channel_en[7:0]	255	
96	Channel_en[15:8]	255	
97	Channel_en[18:16]	3	7
98		0	Do not change
99		0	Do not change
100		0	Do not change
101	Temp[7:0]	0	Do not change
102	Temp[15:8]	0	Do not change
103		136	64
104		136	102
105		96	68
106		96	Do not change
107		96	Do not change
108		96	228
109		64	210

Address	Register Name(s)	Default Value	Fixed Value(1)
110		64	Do not change
111		64	Do not change
112	Vlevel_s2_ex[6:0]	64	
113	Vlevel_s3_ex[6:0]	64	
114	Vlevel_s2[6:0]	64	
115	Vlevel_s3[6:0]	64	
116		96	91
117		96	91
118		96	Do not change
119		96	Do not change
120		96	Do not change
121		255	47
122		255	Do not change
123		64	102
124		0	Do not change
125		0	Do not change
126	ADC_gain[5:0]	32	
127		32	Do not change

(1) Addresses with a fixed value other than the startup value need to be set to the fixed value after startup.

9 Application Information

9.1 Cover Glass

The cover glass of the CMV20000 has following specifications:

- Reflection(abs) <= 1.5% @ 400 – 900 nm (per surface), Angle Off Interest = 15º
- 2 sides AR-coated

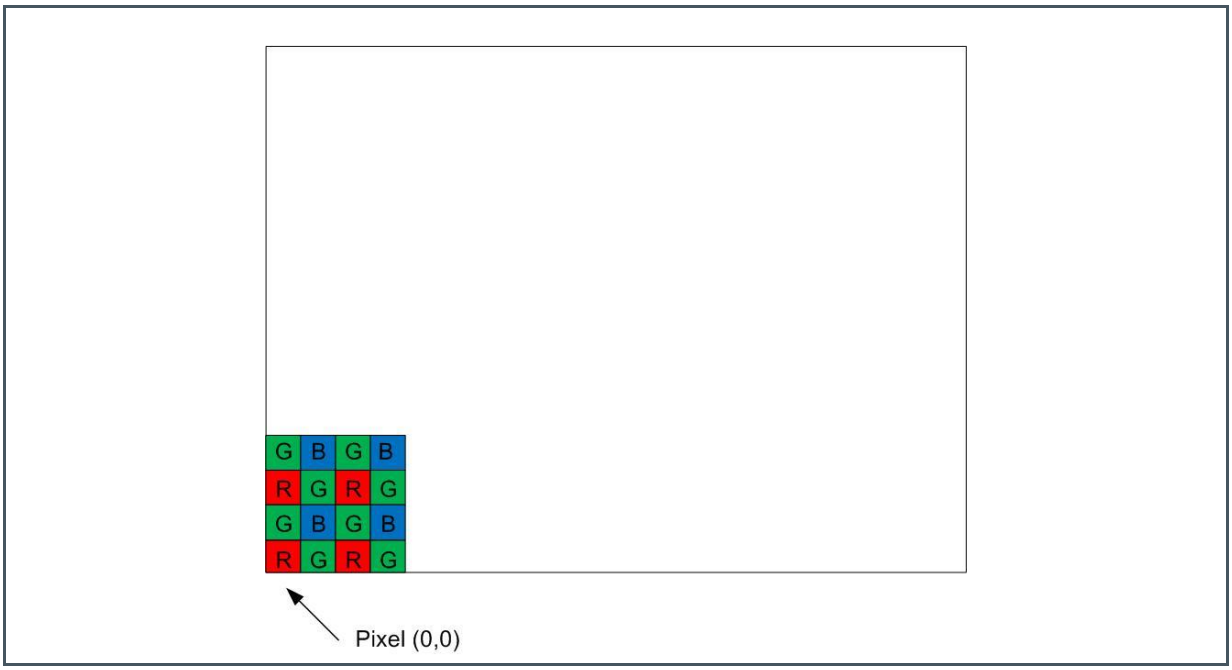
When a color sensor is used an IR-cutoff filter should be placed in the optical path of the sensor.

9.2 Color Filter

When a color version of the CMV20000 is used, the color filters are applied in a Bayer pattern. The color version of the CMV20000 always has micro lenses. The use of an IR cut-off filter in the optical path of the CMV20000 image sensor is necessary to obtain good color separation when using light with an IR component.

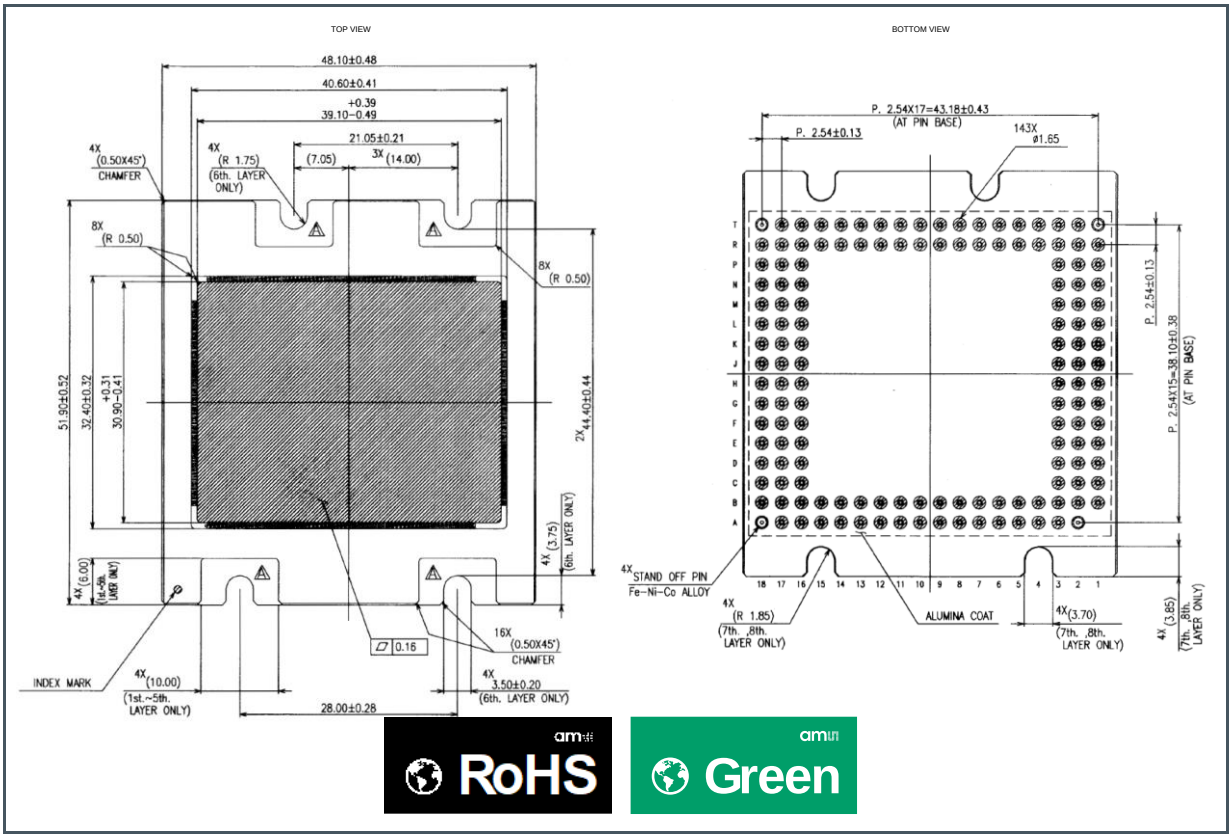
A RGB Bayer pattern is used on the CMV20000 image sensor. The order of the RGB filter can be found in the drawing below.

Figure 60:
RGB Bayer Pattern Order



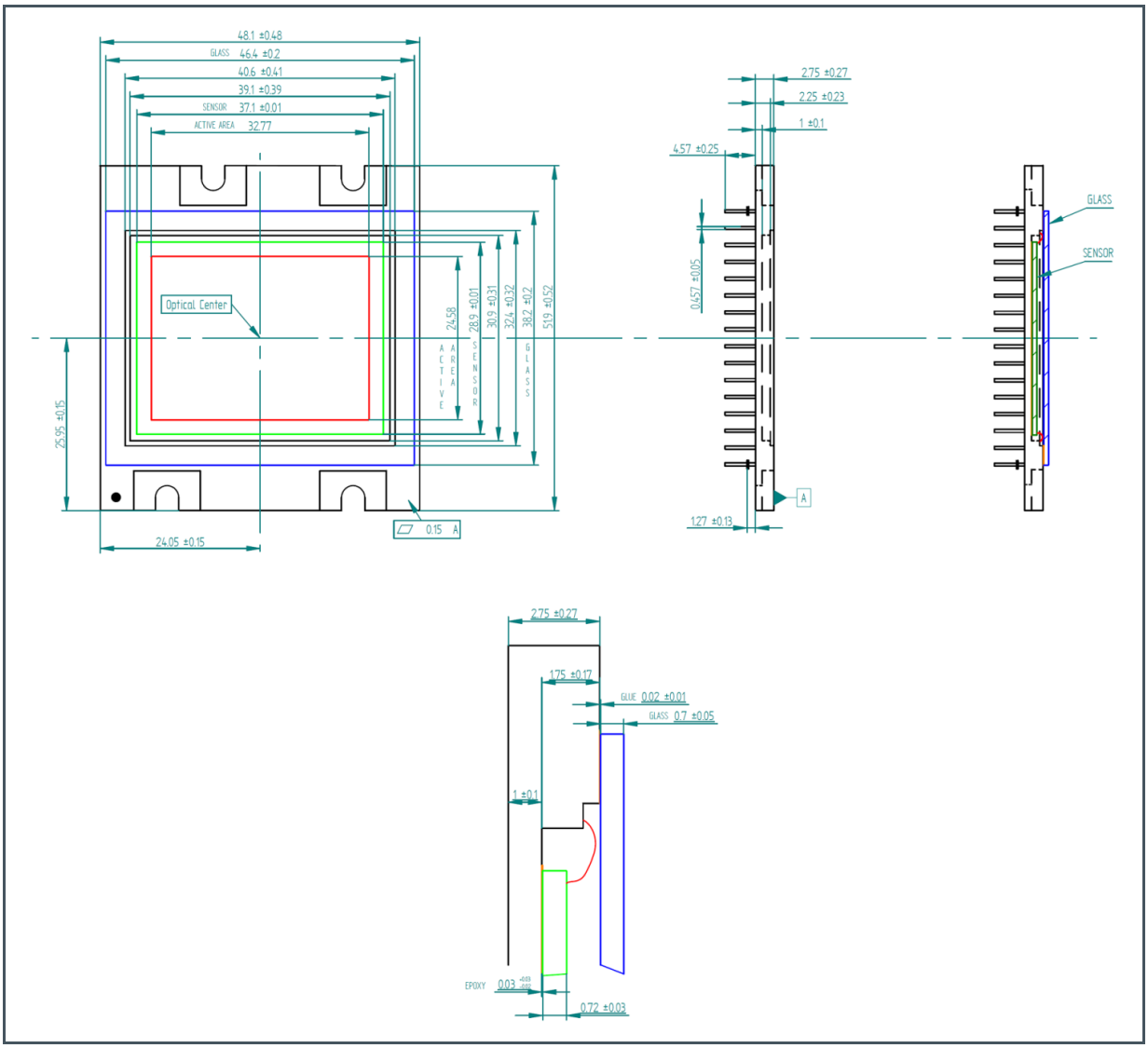
10 Package Drawings & Markings

Figure 61:
Package Outline Drawing



(1) All dimensions are in millimeters
(2) Tilt image sensor: ± 0.05 degree
(3) Rotation image sensor: ± 0.3 degree
(4) Placement image sensor: ±150 µm
(5) Alignment image sensor to the top of the package: 1 mm ± 0.13 mm
(6) Pin alignment tolerances are specified as 1%, however tolerances measured are 0.18% max

Figure 62:
Assembly Outline Drawing



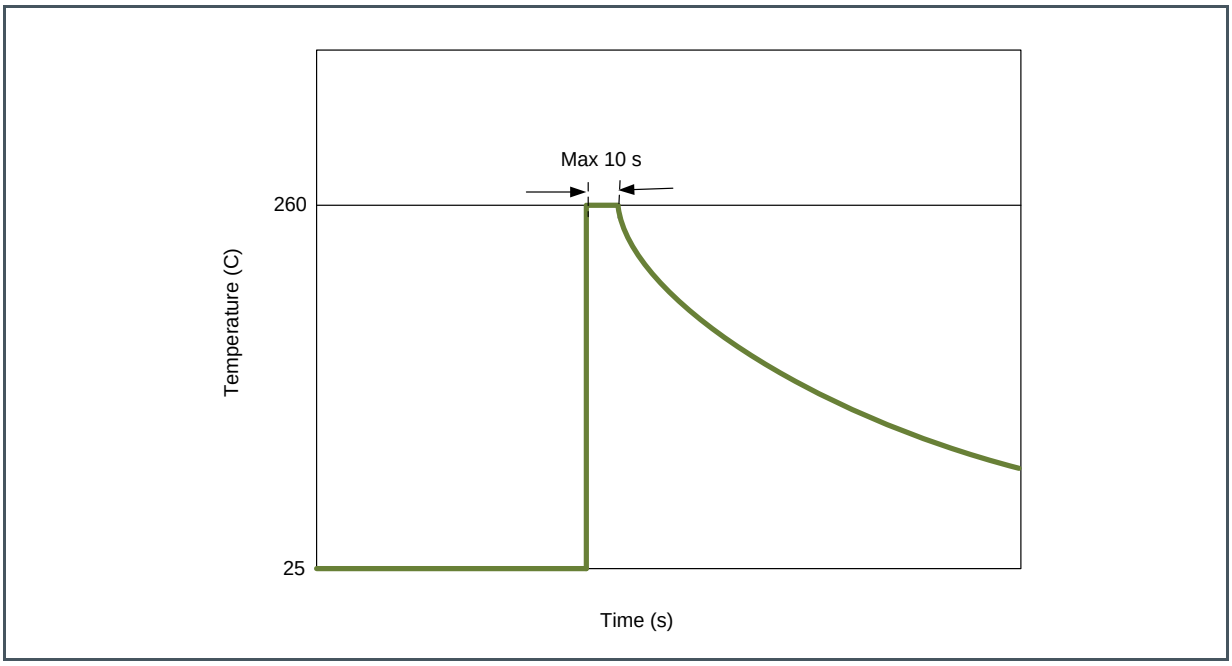
11 Soldering & Handling Information

11.1 Soldering

Wave Soldering

Wave soldering is possible but not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. See the figure below for the wave soldering profile.

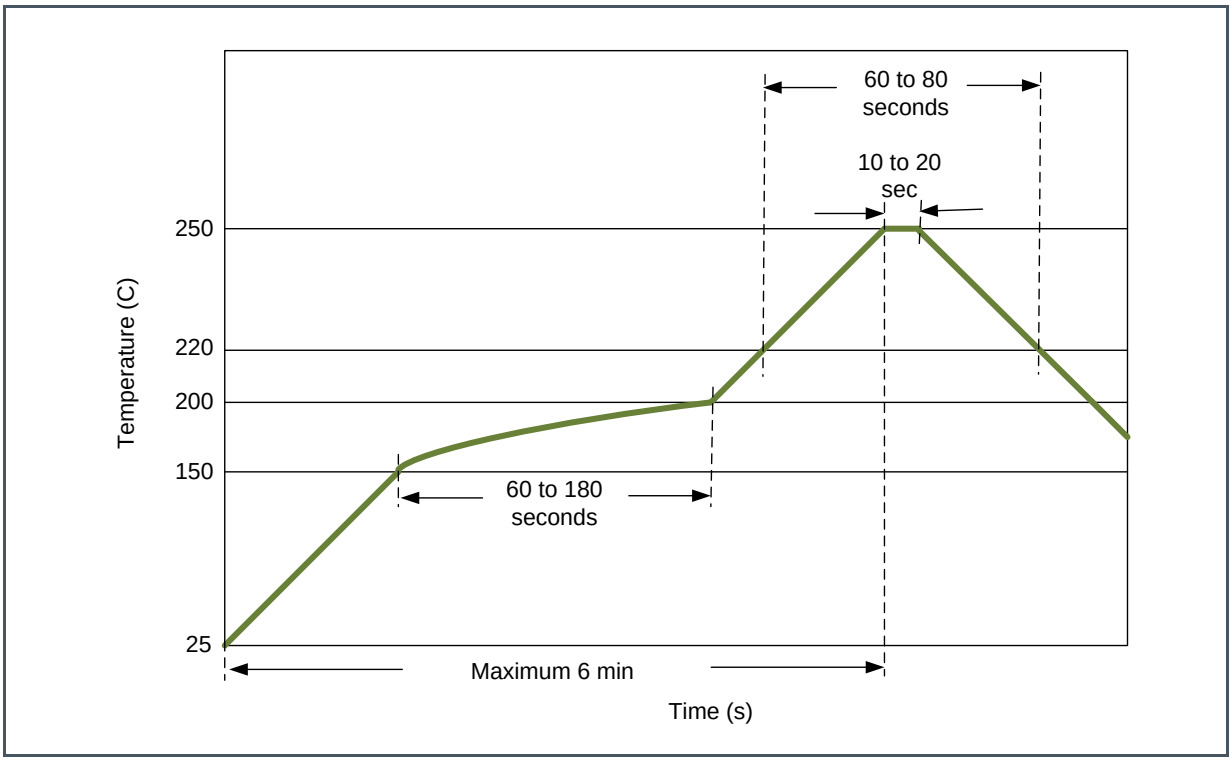
Figure 63:
Wave Soldering Profile



Reflow Soldering

The figure below shows the maximum recommended thermal profile for a reflow soldering system. If the temperature/time profile exceeds these recommendations, damage to the image sensor can occur.

Figure 64:
Solder Reflow Profile Graph



Soldering Recommendations

Image sensors with color filter arrays (CFA) and micro-lenses are especially sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. Best solution will be flow soldering or manual soldering of a socket (through hole or BGA) and plug in the sensor at latest stage of the assembly/test process.

11.2 Handling

General application note AN03 contains more details and procedures.

ESD

The following are the recommended minimum ESD requirements when handling image sensors.

- Ground workspace (tables, floors…)
- Ground handling personnel (wrist straps, special footwear…)
- Minimize static charging (control humidity, use ionized air, wear gloves…)

Glass Cleaning

When cleaning of the cover glass is needed we recommend the following two methods.

- Blowing off the particles with ionized nitrogen
- Wipe clean using IPA (isopropyl alcohol) and ESD protective wipes.

Image Sensor Storing

Image sensors should be stored under the following conditions

- Dust free
- Avoid radiation, electromagnetic fields, ESD, mechanical stress
- See section 4 for storage limits

Excessive Light

Excessive light falling on the sensor can cause heating up the micro lenses and color filters. This heat can cause deforming of the lenses and/or deterioration of the lenses and color filters by making them more opaque, increasing the heat up even more. Avoid shining high intensity light upon the sensors for extended periods of time. In case of lasers, they can cause heat up but can also damage the silicon die itself.

12 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Changes from previous version to current revision v2-00	Page
Update to **ams** template	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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