IR3899A IPOL

9 A single-voltage synchronous Buck regulator

Features

- Single 4.3 V to 17 V application
- Precision Reference Voltage (0.6 V +/-0.5%)
- Enhanced Fast COT engine stable with Ceramic Output Capacitors and No External Compensation
- Optional Forced Continuous Conduction Mode or Diode Emulation for Enhanced Light Load Efficiency
- Programmable Switching Frequency from 600 kHz to 2 MHz
- Enable input with Voltage Monitoring Capability & Power Good Output
- Monotonic Start-Up with 2 ms soft start time & Enhanced Pre-Bias Start up
- Thermally compensated Internal Over Current Protection with Two Selectable Settings
- Thermal Shut Down
- Operating Junction Temp: -40 °C < T_j < 125 °C
- Small Size: 4 mm x 5 mm PQFN
- Halogen-free and RoHS Compliant

Potential applications

- Server Applications
- Storage Applications
- Telecom & Datacom Applications
- Distributed Point of Load Power Architectures

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

The IR3899A is an easy-to-use, fully integrated dc - dc Buck regulator. The onboard PWM controller and MOSFETs with integrated bootstrap diode make IR3899A a small footprint solution, providing high-efficiency power delivery. Furthermore, it uses a fast Constant On-Time (COT) control scheme, which simplifies design efforts and provides fast control response.

The IR3899A has an internal low dropout voltage regulator, allowing operation with a single supply. The IR3899A is a versatile regulator, offering programmable switching frequency from 600 kHz to 2 MHz, two selectable current limits, Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DEM) operation.

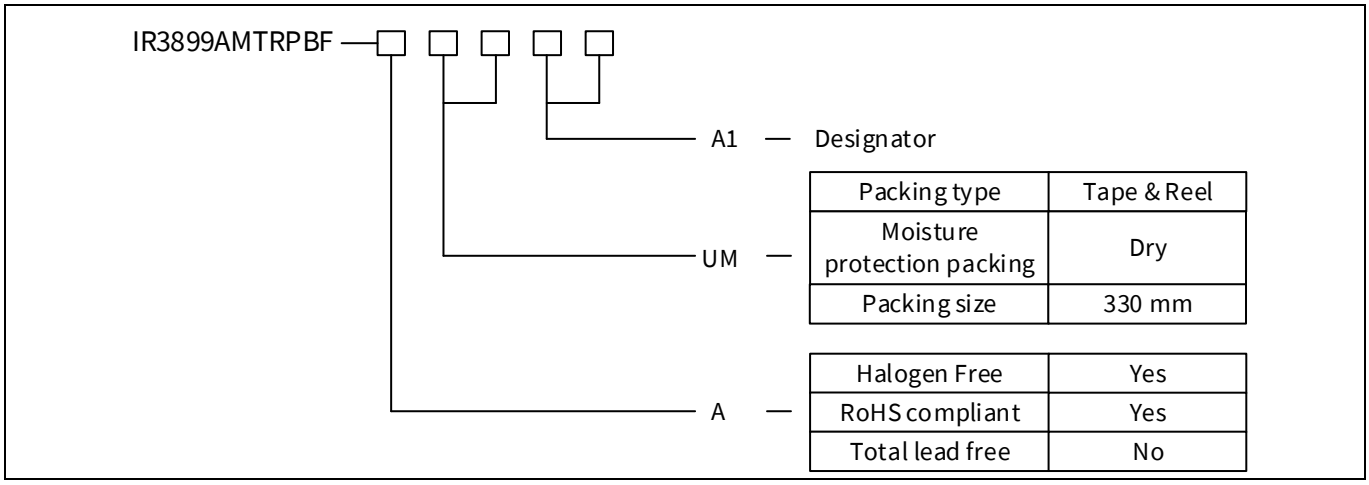
It also features important protection functions, such as pre-bias start-up, thermally compensated current limits, over voltage and under voltage protection, and thermal shutdown to give required system level security in the event of fault conditions.

Table of contents

1 Ordering information

1. Ordering Information

Base Part Number	Package Type	Standard Pack Form and Qty		Orderable Part Number
IR3899AMTRPBF	PQFN 4 mm x 5 mm	Tape and Reel	4000	IR3899AMTRPBFAUMA1



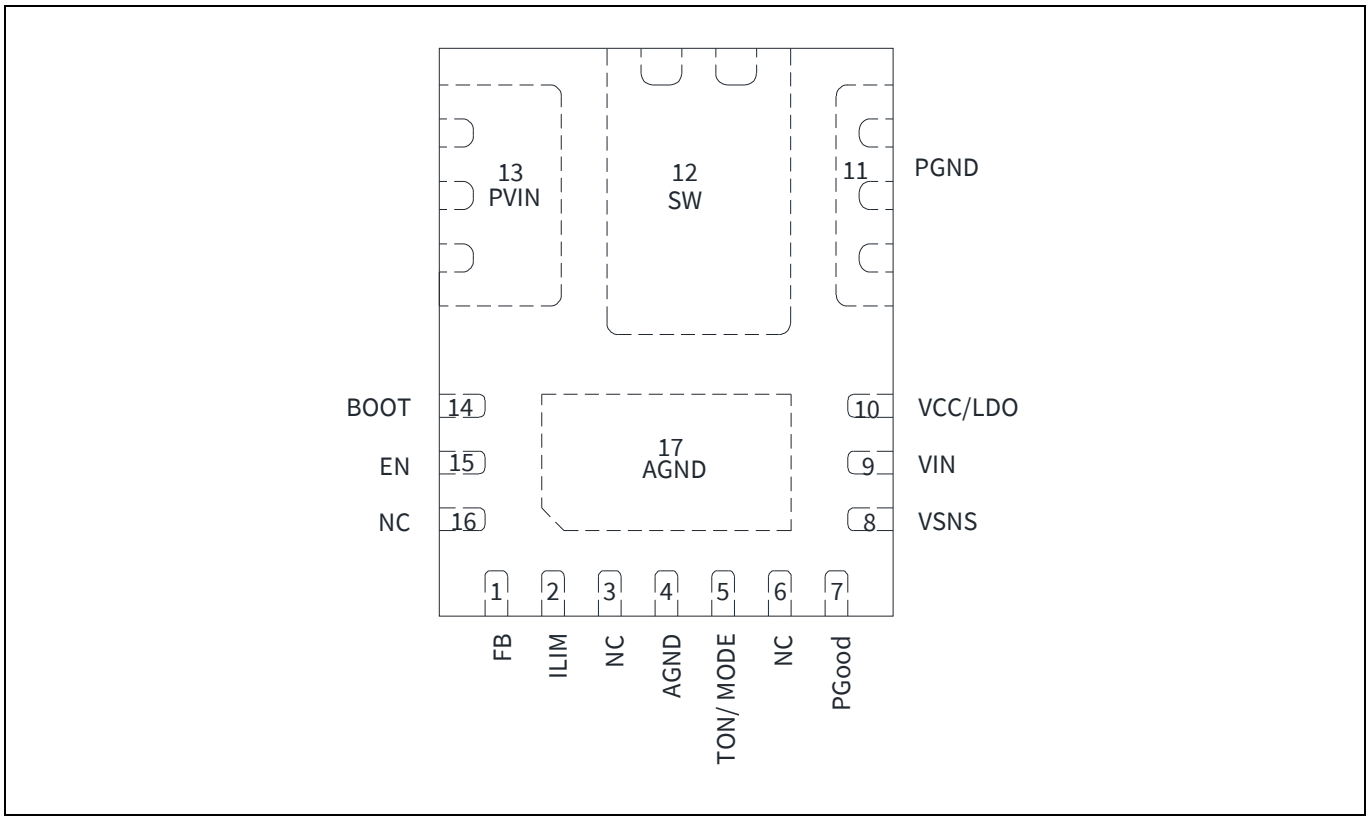


Figure 1 Package Top View

2 Functional block diagram

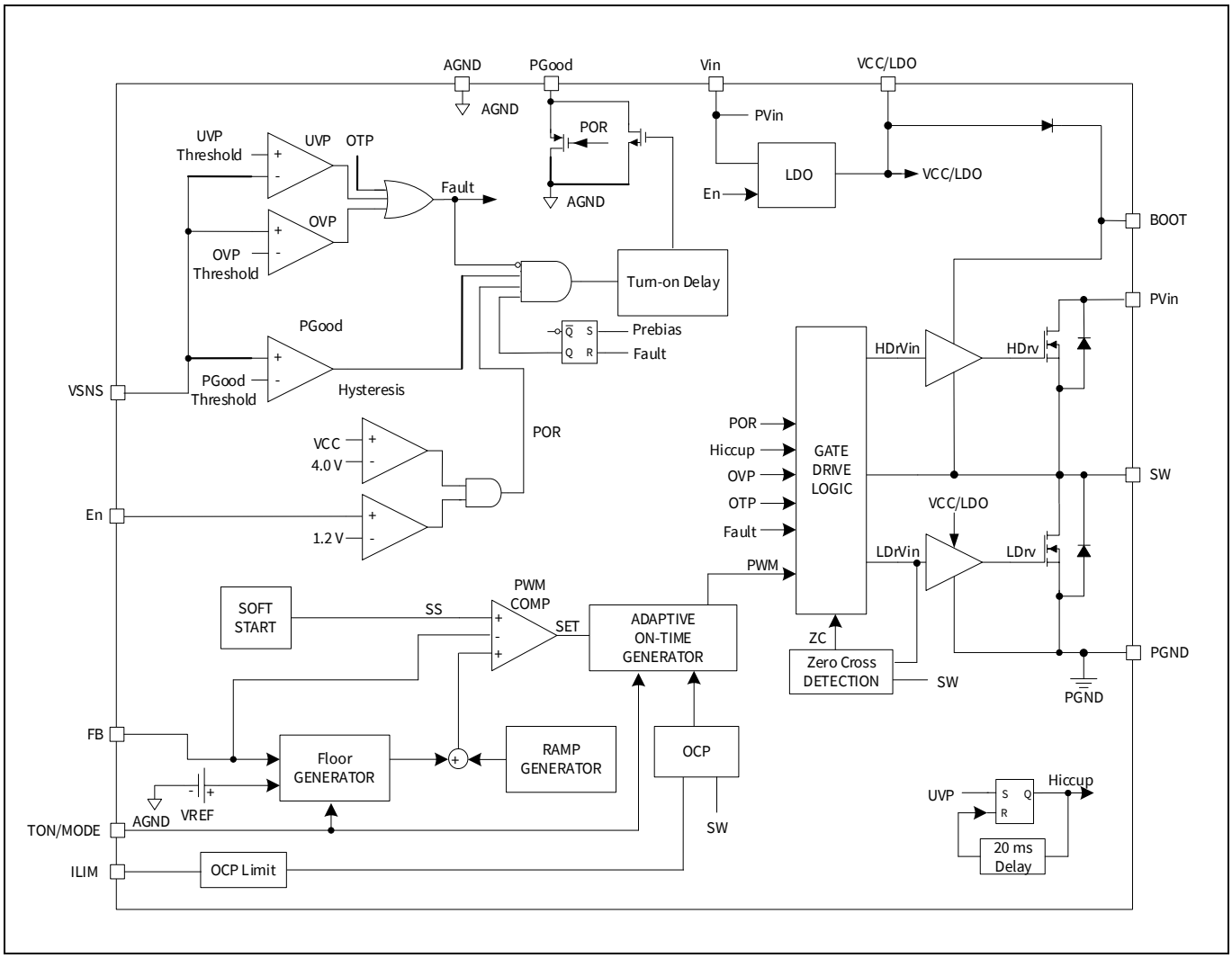


Figure 2 Block diagram

3 Typical application diagram

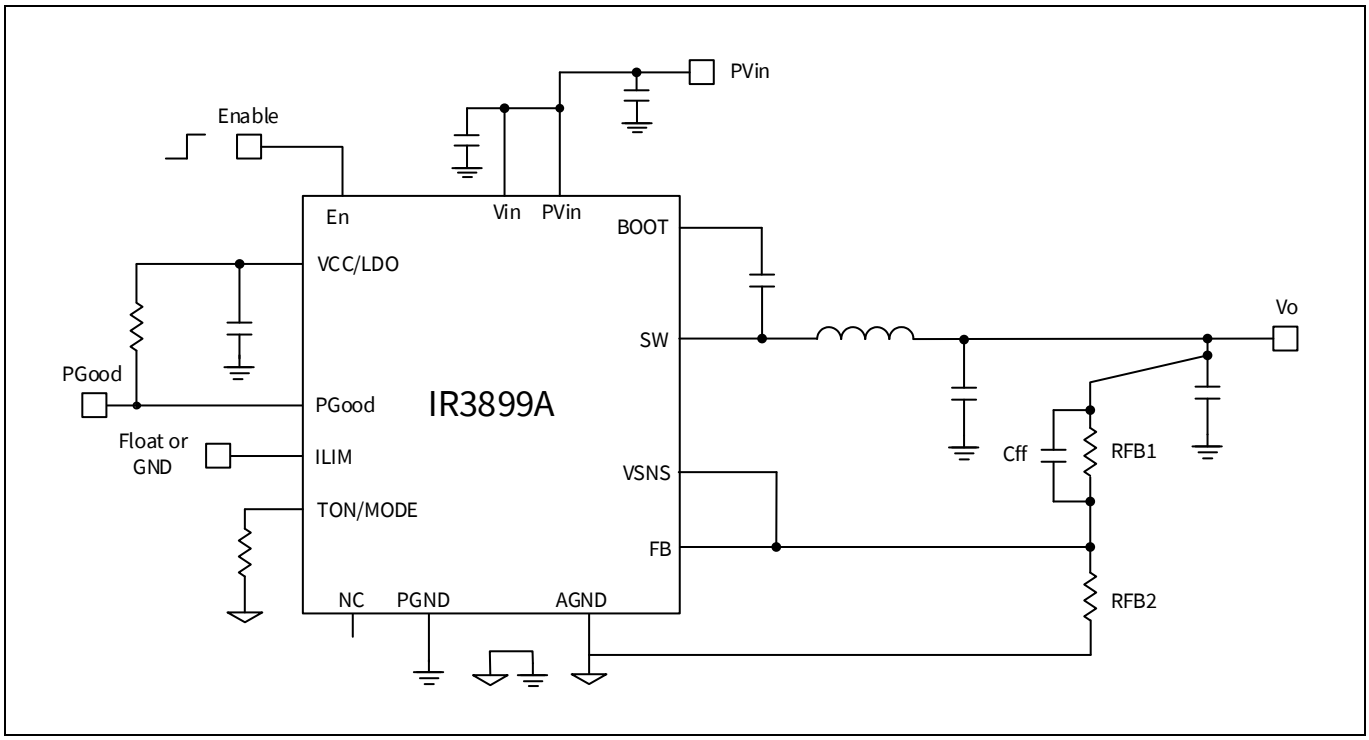


Figure 3 IR3899A basic application circuit

4 Pin descriptions

Note: *I = Input, O = Output*

Pin#	Pin Name	I/O	Type	Pin Description
1	FB	I	Analog	Output voltage feedback pin. Connect this pin to the output of the regulator via a resistor divider to set the output voltage.
2	ILIM	I	Analog	Shorting to GND or floating the pin sets the Over Current Protection (OCP) limit. Two User selectable OCP limits are available.
3, 6, 16	NC	-	No connect	This pin can be left floating. Note: Pin 6 is internally connected and should either be left floating or can be connected to VCC/LDO.
4, 17	AGND	-	Ground	Signal ground for the internal reference voltage and control circuitry. AGND and PGND are not internally connected. AGND and PGND must be connected on the PCB with a single ground connection.
5	TON/MODE	I	Analog	Multi-function pin. This pin sets the switching frequency to 1 of 8 settings and sets the mode of operation to FCCM or DEM by connecting a resistor to ground.
7	PGood	O	Analog	Power Good status output pin is open drain. Connect a pull up resistor from this pin to VCC/LDO or to an external bias voltage, e.g., 3.3 V.
8	VSNS	I	Analog	Sense pin for over voltage protection and PGood. Tie this pin to Vout using a resistor divider. Alternatively, tie this pin to the FB pin directly.
9	Vin	I	Power	Vin is the input voltage for the Internal LDO and it should always be connected to PVin; also forms input to the feedforward block. A 4.7 µF capacitor should be connected between this pin and PGND.
10	VCC/LDO	I	Power	Output of the internal LDO. A ceramic capacitor valued between 2.2 µF and 10 µF is recommended for use between VCC/LDO and the Power ground (PGND).
11	PGND	-	Ground	Power ground. This pin should be connected to the system's power ground plane. Bypass capacitors between PVin and PGND should be connected very close to these pins.
12	SW	O	Power	Switch node. This pin is connected to the output inductor.
13	PVin	I	Power	Input voltage for power stage. Bypass capacitors between PVin and PGND should be connected very close to these pins.
14	BOOT	I	Analog	Supply voltage for the high side driver. Connect this pin to the SW pin through a bootstrap capacitor.
15	En	I	Analog	Enable pin to turn the IC on and off.

5 Absolute maximum ratings

Absolute maximum ratings

Description	Min	Max	Unit	Conditions
PVin, Vin, En to PGND	-0.3	25	V	Note **1**
PVin to SW	-0.3 V(dc), below -5 V for 5 ns	25	V	
VCC/LDO to PGND	-0.3	6	V	Note **1**
BOOT to PGND	-0.3 V(dc), below -0.3 V for 5 ns	29	V	Note **1**
SW to PGND	-0.3 (dc), below -5 V for 5 ns	25	V	Note **1**
BOOT to SW	-0.3	6	V	
ILIM, FB, PGood, TON/MODE and VSNS to AGND	-0.3	6	V	Note **1**
PGND to AGND	-0.3	0.3	V	
Storage Temperature Range	-55	150	°C	
Junction Temperature Range	-40	150	°C	

Note:

1. PGND and AGND pins are connected together

Attention: ***Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

6 Thermal characteristics

6.1 Thermal Characteristics

Description	Symbol	Values	Test Conditions
Junction to Ambient Thermal Resistance	θ_{JA}	32 °C/W	
Junction to PCB Thermal Resistance	$\theta_{JC\text{-}PCB}$	2 °C/W	

7 Electrical specifications

7.1 Recommended operating conditions

Description	Min	Max	Unit	Note
PV_{in} Voltage Range	4.5	17	V	Note **2**, Note **3 & 6**
Typical Output Voltage Range	0.6	6	V	Note **4**, Note **5**
Continuous Output Current Range		9	A	Note **5**
Typical Switching Frequency	600	2000	kHz	Note **6**
Operating Junction Temperature	-40	125	°C	

Note:

2. *A common practice is to have 20% margin on the maximum SW node voltage in the design. A 2Ω resistor in series with the BOOT pin is recommended for PVin ≥ 13.2 V to ensure the maximum SW node spike voltage does not exceed 20 V. Alternatively, an RC snubber can be used at the SW node to reduce the SW node spike.*
3. *For single-rail applications with PV_{in} = V_{in} = 4.3 V-5.4 V, the internal LDO may enter dropout mode. OCP limits can be reduced due to the lower VCC voltage.*
4. *The maximum output voltage is limited by the minimum off-time. Please refer to **Section 12.13** for details. Also note that OCP limit may be degraded when off-time is close to the minimum off-time.*
5. *Maximum output current capability can be reduced at elevated ambient temperatures. Lower VCC voltage can result in higher $R_{DS(ON)}$ and therefore require more thermal derating.*
6. *The maximum LDO output current must be limited to 50 mA or less for operations requiring the full operating temperature range of -40 °C ≤ T_J ≤ 125 °C. Thermal derating may be needed for operation at elevated ambient temperatures to ensure the junction temperature remains within the recommended operating range.*

7.2 Electrical characteristics

Note: Unless otherwise specified, the specifications apply over 4.5 V ≤ Vin = PVin ≤ 17 V, 0 °C < T_J < 125 °C. Typical values are specified at Ta = 25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Stage						
Top Switch	$R_{DS\ (on)\_Top}$	V_{BOOT} – V_{SW} = 5.0 V, T_j = 25 °C		21		mΩ
Bottom Switch	$R_{DS\ (on)\_Bot}$	VCC = 5.0 V, T_j = 25 °C		9		
Bootstrap Forward Voltage		I(Boot) = 25 mA		370	600	mV
SW float voltage	V_{SW}	En = 0 V			300	mV
		En = high, No Switching			300	
Dead Band Time	T_{db}	SW node rising edge, Note 7		10		ns
		SW node falling edge, Note 7		10		ns
Supply Current						
Vin Supply Current (standby)	$I_{in\ (Standby)}$	En = Low, No Switching		4	10	µA
Vin Supply Current (static)	$I_{in\ (Static)}$	En = 2 V, No Switching		2.3	4	mA
Soft Start						
Soft Start time	SS time		1.4	2	3	ms
Feedback Voltage						
Feedback Voltage	V_{FB}			0.6		V
Accuracy		0 °C < T_j < 85 °C, Note 8	-0.5		+0.5	%
		-40 °C < T_j < 125 °C, Note 8	-1		1	
V_{FB} Input Current	IV_{FB}	V_{FB} = 0.6 V, T_j = 25 °C	-0.15	0	+0.15	µA
On-Time Timer Control						
On Time	T_{on}	Vin = 12 V, Vo = 1 V, TON/MODE = 0 kΩ, 10.5 kΩ, Note 9		152		ns
		Vin = 12 V, Vo = 1 V, TON/MODE = 1.5 kΩ, 12.1 kΩ, Note 9		114		
		Vin = 12 V, Vo =1 V, TON/MODE = 2.49 kΩ, 14 kΩ, Note 9		91.5		
		Vin = 12 V, Vo = 1 V, TON/MODE = 3.48 kΩ, 16.2 kΩ, Note 9		77		
		Vin = 12 V, Vo = 1 V, TON/MODE = 4.53 kΩ, 18.7 kΩ, Note 9		66.5		
		Vin = 12 V, Vo = 1 V, TON/MODE = 5.76 kΩ, 21.5 kΩ, Note 9		58.5		
		Vin = 12 V, Vo = 1 V, TON/MODE = 7.32 kΩ, 24.9 kΩ, Note 9		52		
		Vin = 12 V, Vo = 1 V, TON/MODE = 8.87 kΩ, 28.7 kΩ, Note 9		47		
		Vin = 12 V, Vo = 1 V, TON/MODE = Floating, Note 9		114		
Minimum On-Time	$T_{on\ (Min)}$	Vin = 12 V, Vo = 0 V		23	32	ns
Minimum Off-Time	$T_{off\ (Min)}$	T_j = 25 °C, V_{FB} = 0 V		270	360	ns

Electrical specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC LDO Output						
Output Voltage	VCC	5.5 V ≤ Vin ≤ 17 V, when Icc = 50 mA, Cload = 2.2 µF	4.7	5.0	5.3	V
VCC Dropout	VCC_drop	Vin = 4.3 V, Icc = 50 mA, Cload = 2.2 µF			300	mV
Short Circuit Current	I_{short}	5.5 V ≤ Vin ≤ 17 V		90		mA
Under Voltage Lockout						
VCC-Start Threshold	Vcc_UVLO_Start	VCC Rising Trip Level	3.8	4.0	4.2	V
VCC-Stop Threshold	Vcc_UVLO_Stop	VCC Falling Trip Level	3.6	3.8	4.0	
Enable-Start-Threshold	En_UVLO_Start	ramping up	1.14	1.2	1.36	V
Enable-Stop-Threshold	En_UVLO_Stop	ramping down	0.9	1	1.06	
Input Impedance	R_{EN}		500	1000	1500	kΩ
Over Current Limit						
Current Limit Threshold (Valley Current)	Ioc	T_j = 25 °C, VCC = 5.0 V, ILIM = GND	6.8	9.0	10.5	A
		T_j = 25 °C, VCC = 5.0 V, ILIM = Floating	10	12.7	15	
Over Voltage Protection						
OVP Trip Threshold	OVP_Vth	VSNS Rising	115	121	125	% Vref
		VSNS Falling, OVP hysteresis	110	115	120	
OVP Protection Delay	OVP_Tdly			5		µs
Under Voltage Protection						
UVP Trip Threshold	UVP_Vth	VSNS Falling	65	70	75	% Vref
UVP Protection Delay	UVP_Tdly			4		µs
Hiccup Blanking Time	Tblk_Hiccup			20		ms
Power Good						
Pgood Turn on Threshold	VPG (upper)	VSNS Rising	85	91	95	% Vref
Pgood Turn off Threshold	VPG (lower)	VSNS Falling	80	84	90	% Vref
Pgood Sink Current	I_{PG}	PGood = 0.5 V, En = 2 V	2.5	5		mA
Pgood Voltage Low	$V_{PG\ (low)}$	Vin = VCC = 0 V, Rpull-up = 50 kΩ to 3.3 V		0.3	0.5	V
Pgood Turn on Delay	$V_{PG\ (on)\_Dly}$	VSNS Rising, see VPG (upper)		2.5		ms
Pgood Comparator Delay	$V_{PG\ (comp)\_Dly}$	VSNS < VPG (lower) or VSNS > VPG (upper)	1	2	3.5	µs
Pgood Open Drain Leakage Current		PGood = 3.3 V			1	µA
Thermal Shutdown						
Thermal Shutdown		Note 7		140		°C
Hysteresis		Note 7		20		

Note:

7. *Guaranteed by construction and not tested in production.*
8. *Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.*
9. *Ton is trimmed so that the target switching frequency is achieved at around 4 A load current.*

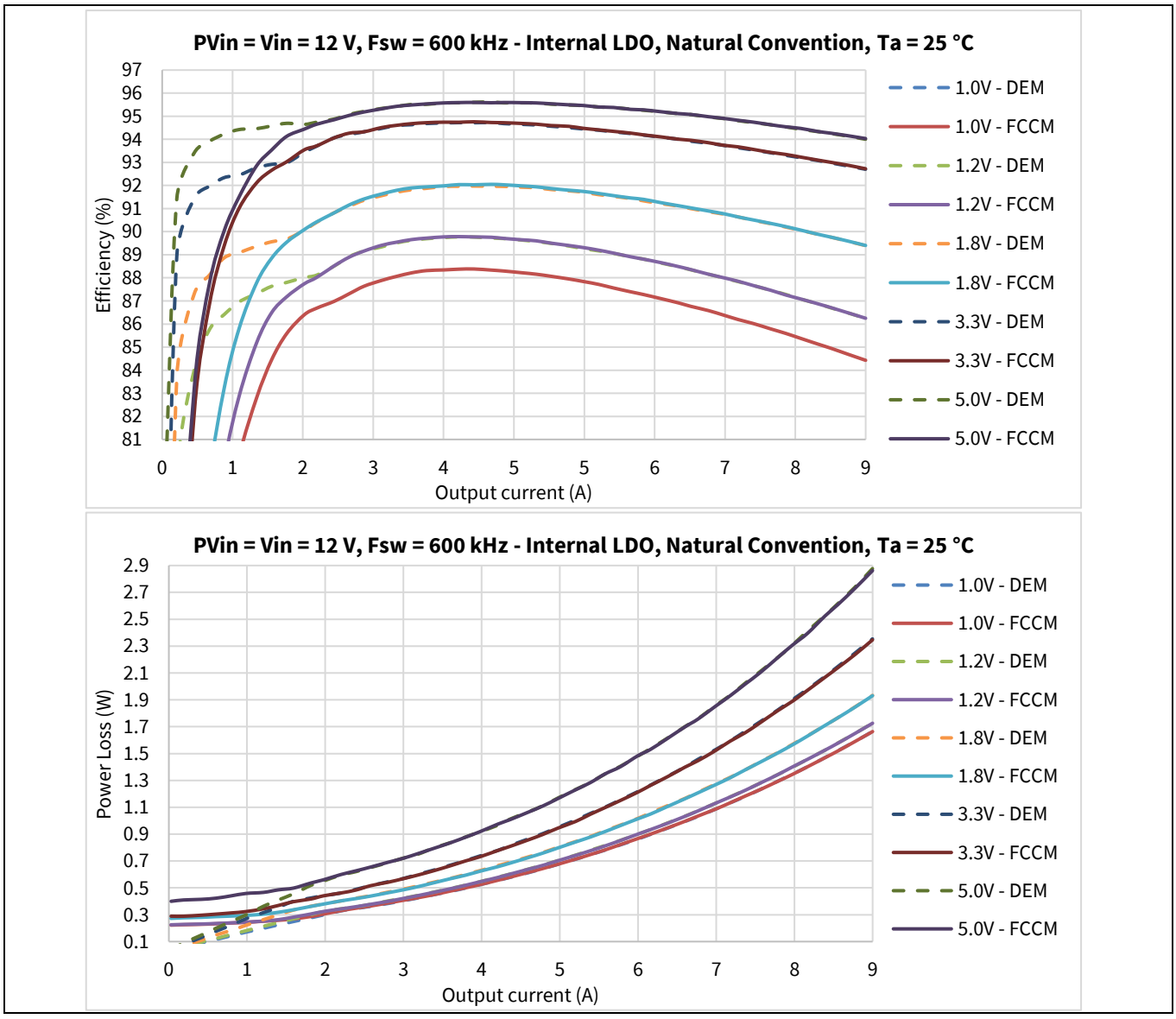
8 Typical efficiency and power loss curves

8.1 $PV_{in} = V_{in} = 12$ V, $F_{sw} = 600$ kHz

$PV_{in} = V_{in} = 12$ V, VCC = Internal LDO, $I_o = 0$ A - 9 A, $F_{sw} = 600$ kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include losses of the IR3899A, inductor losses, losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Table 1 Inductors for $PV_{in} = V_{in} = 12$ V, $F_s = 600$ kHz

Vout (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
1.0	360 nH	CMLE104T-R36MS	0.76	11.15 x 10.0 x 3.8
1.2	470 nH	CMLB104T-R47MS	1.5	11.15 x 10.0 x 3.8
1.8	680 nH	CMLE104T-R68MS	1.6	11.15 x 10.0 x 3.8
3.3	1000 nH	CMLB104T-1R0MS	3.3	11.15 x 10.0 x 3.8
5.0	1000 nH	CMLB104T-1R0MS	3.3	11.15 x 10.0 x 3.8



9 Thermal de-rating cuves

Measurement is done on IR3899A Evaluation board at 200LFM. The PCB is a 4-layer board with 1.8 oz. copper for top and bottom layers and 2 oz. copper for the inner layers, FR4 material, size 2.2” x 2.6”.

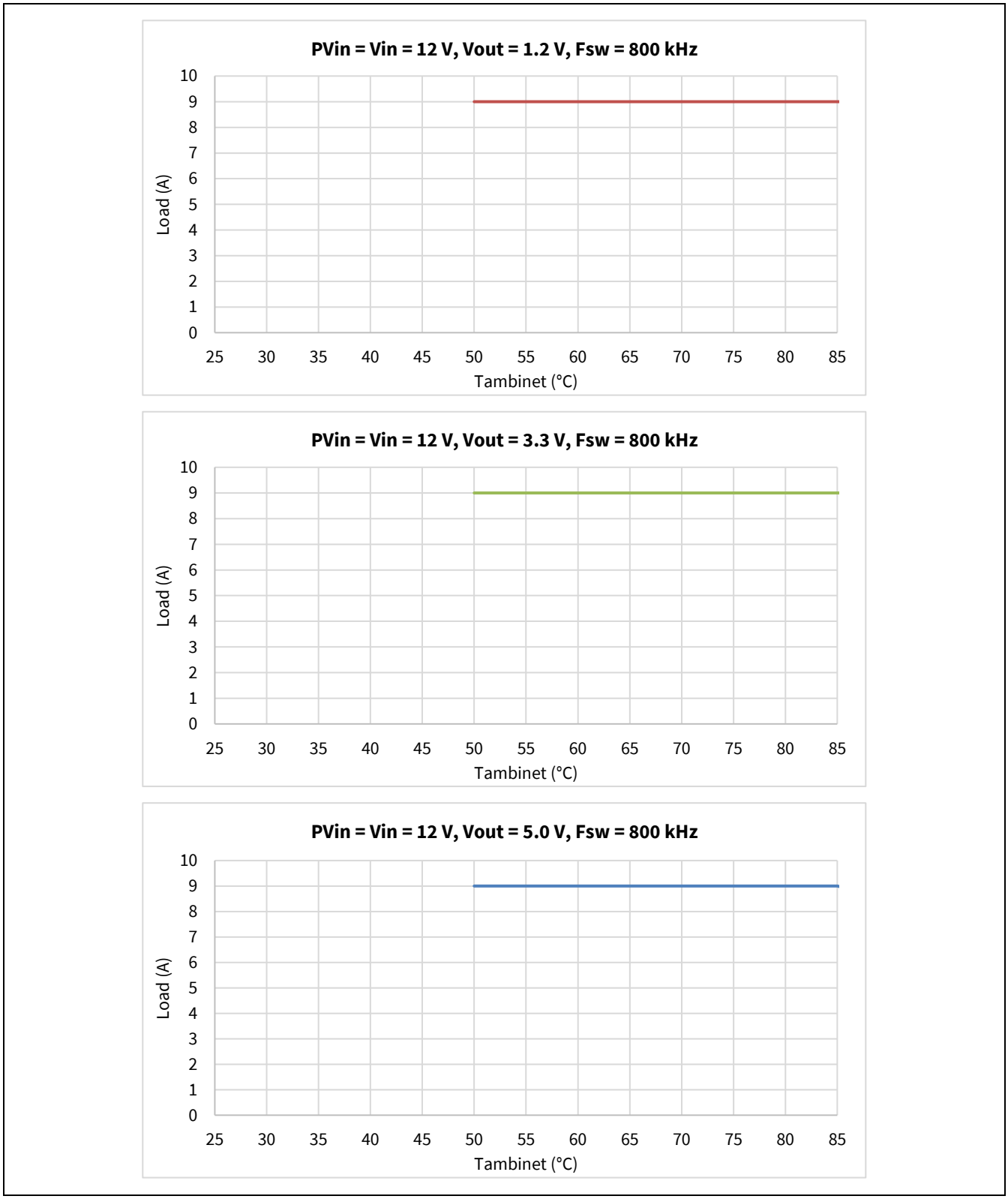
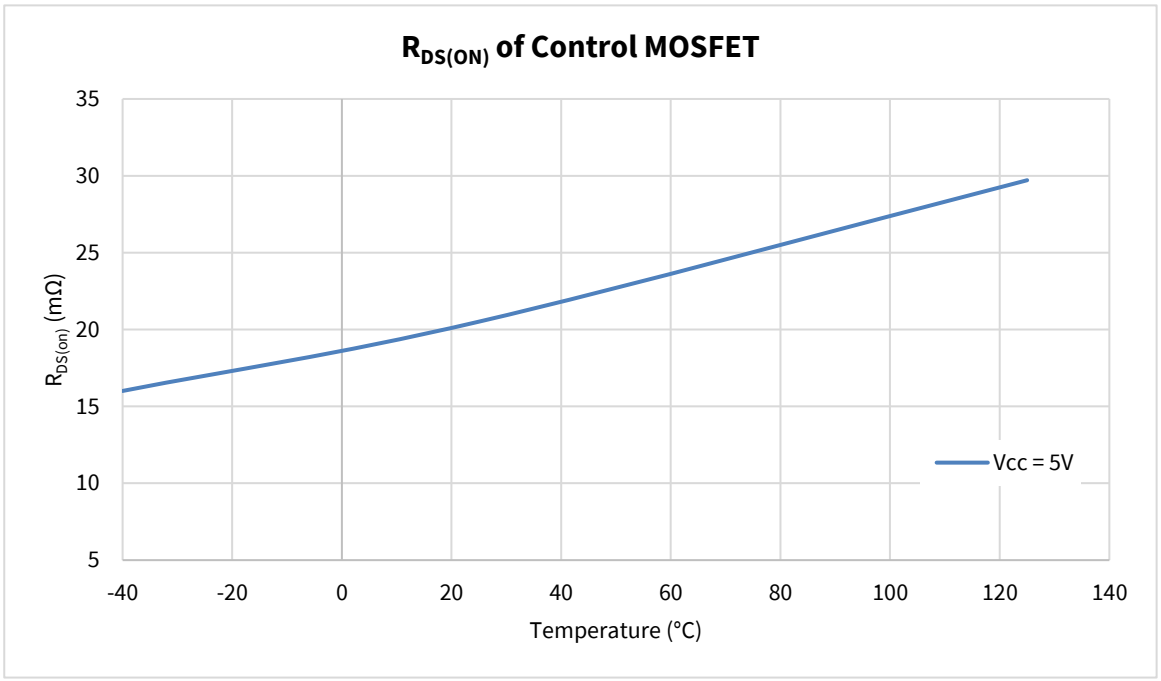


Figure 4 Thermal derating curves, PVin = 12 V, Vout = 1.2 V/3.3 V/5 V, fsw = 800 kHz, VCC = Internal LDO

10 $R_{DS(ON)}$ of MOSFET over temperature



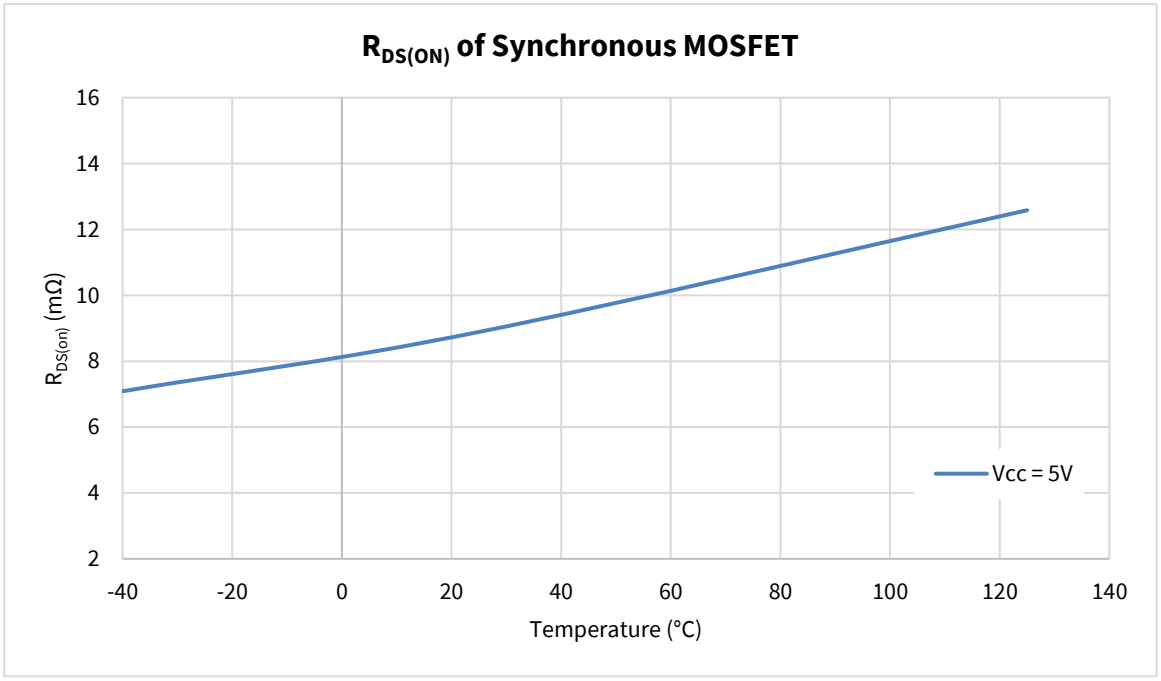
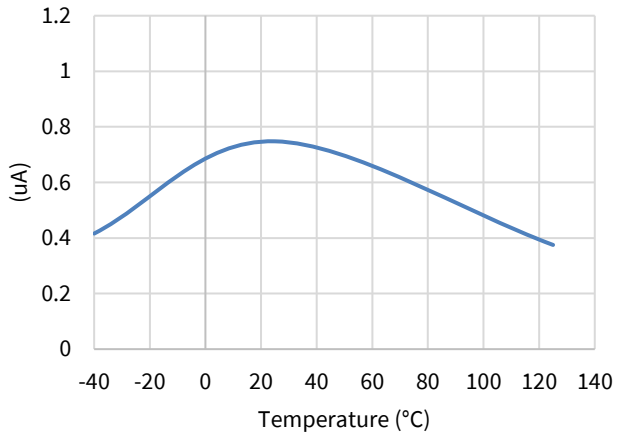


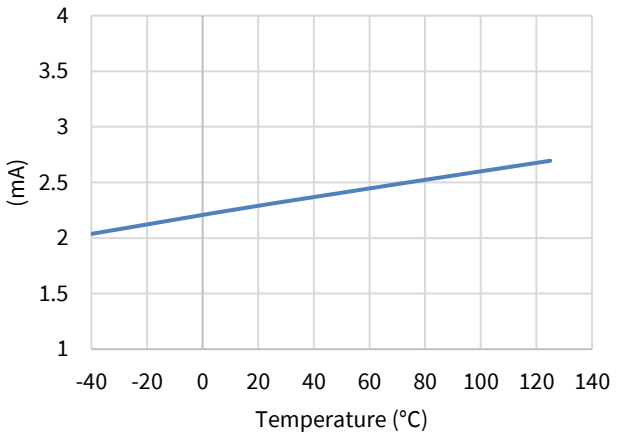
Figure 5 $R_{DS(ON)}$ of MOSFETs over Junction Temperature

11 Typical operating characteristics (-40 °C ≤ T_j ≤ +125 °C)

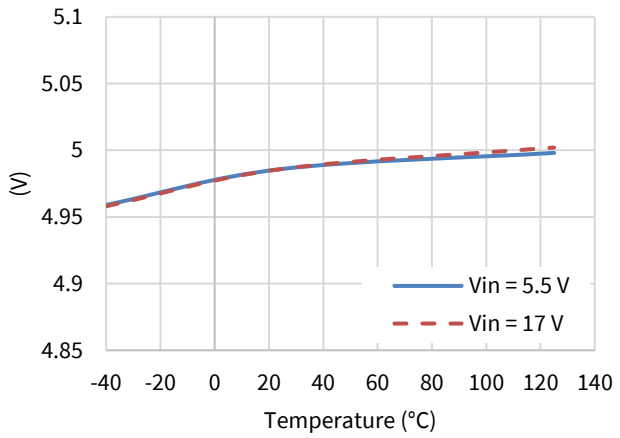
Vin Standby Supply Current



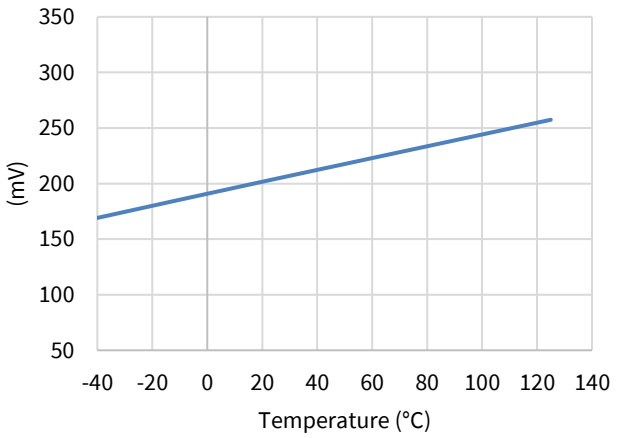
Vin Static Supply Current



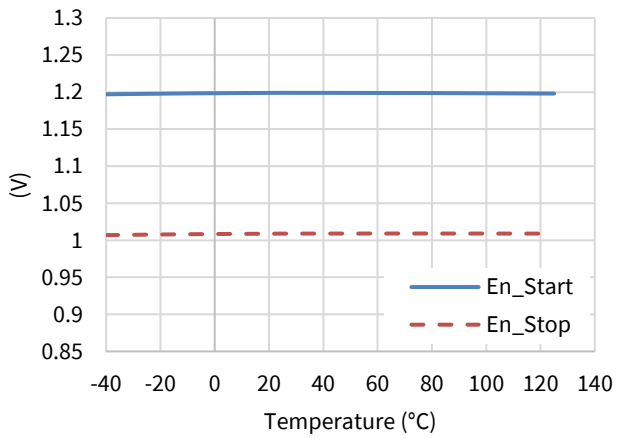
LDO Voltage at Vin = 5.5 V & 17 V, Icc = 50 mA



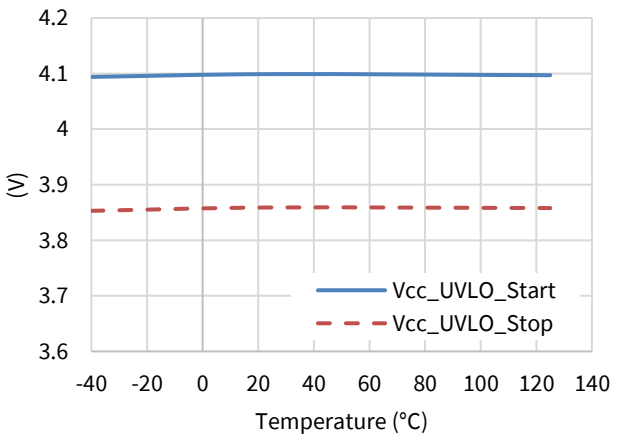
LDO Voltage Drop at Vin = 4.3 V, Icc = 50 mA



Enable_Start and Stop Thresholds



Vcc_UVLO Start and Stop Thresholds



Typical operating characteristics (-40 C ≤ Tj ≤ +125 C)

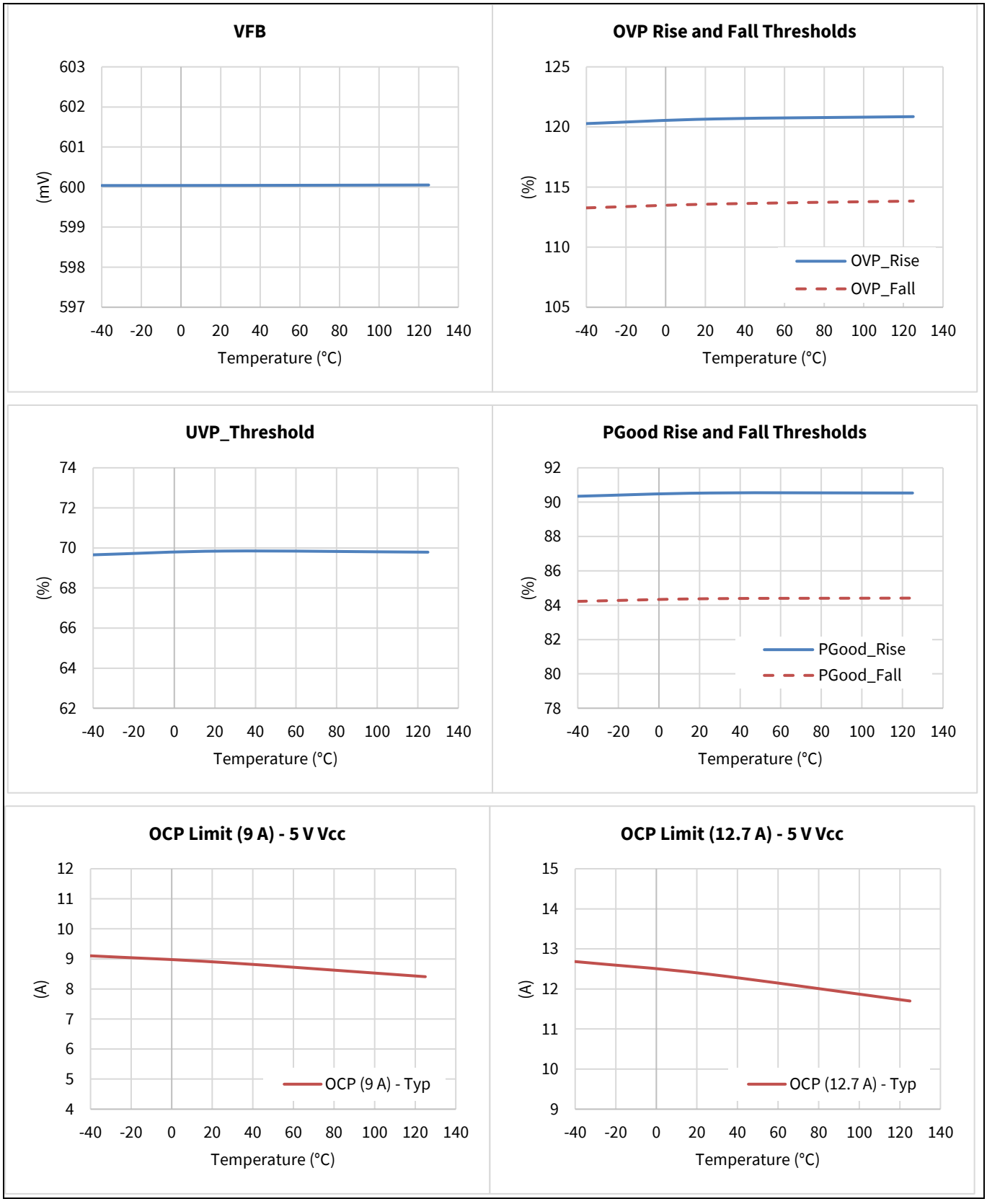


Figure 6 Typical operating characteristics

12 Theory of operation

12.1 Fast Constant On-Time Control

The IR3899A features a proprietary Fast Constant On-Time (COT) Control, which can provide fast load transient response, good output regulation and minimize design effort. Fast COT control compares the output voltage, V_o, to a floor voltage combined with an internal ramp signal. When V_{out} drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internally-compensated error amplifier, which compares Vout with a reference voltage. Compared to the traditional COT control, Fast COT control significantly improves Vout regulation.

12.2 Enable

The EN pin controls the on/off state of the IR3899A. An internal Under Voltage Lock-Out (UVLO) circuit monitors the EN voltage. When the EN voltage is above an internal threshold, the internal LDO starts to ramp up. When the VCC/LDO voltage rises above the VCC_UVLO_Start threshold, the soft-start sequence starts. The EN pin can be configured in three ways, as shown in **Figure 7**. With configuration 2, the Enable signal is derived from the PVin voltage by a resistor divider, REN1 and REN2. By selecting different divider ratios, users can program a UVLO threshold for the bus voltage. This is a very desirable feature because it prevents the IR3899A from operating until PVin is higher than a desired voltage level. For some space-constrained designs, the EN pin can be directly connected to PVin without using the external resistor divider, as shown in Configuration 3. The EN pin should not be left floating. A pull-down resistor in the range of tens of kilohms is recommended. **Figure 8** illustrates the corresponding start-up sequences with three EN configurations.

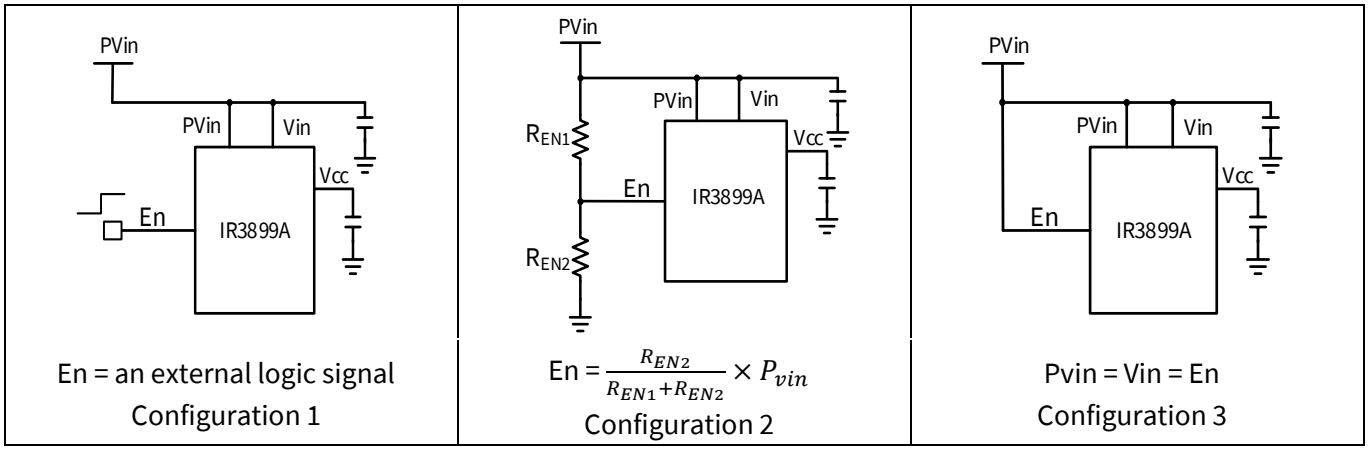
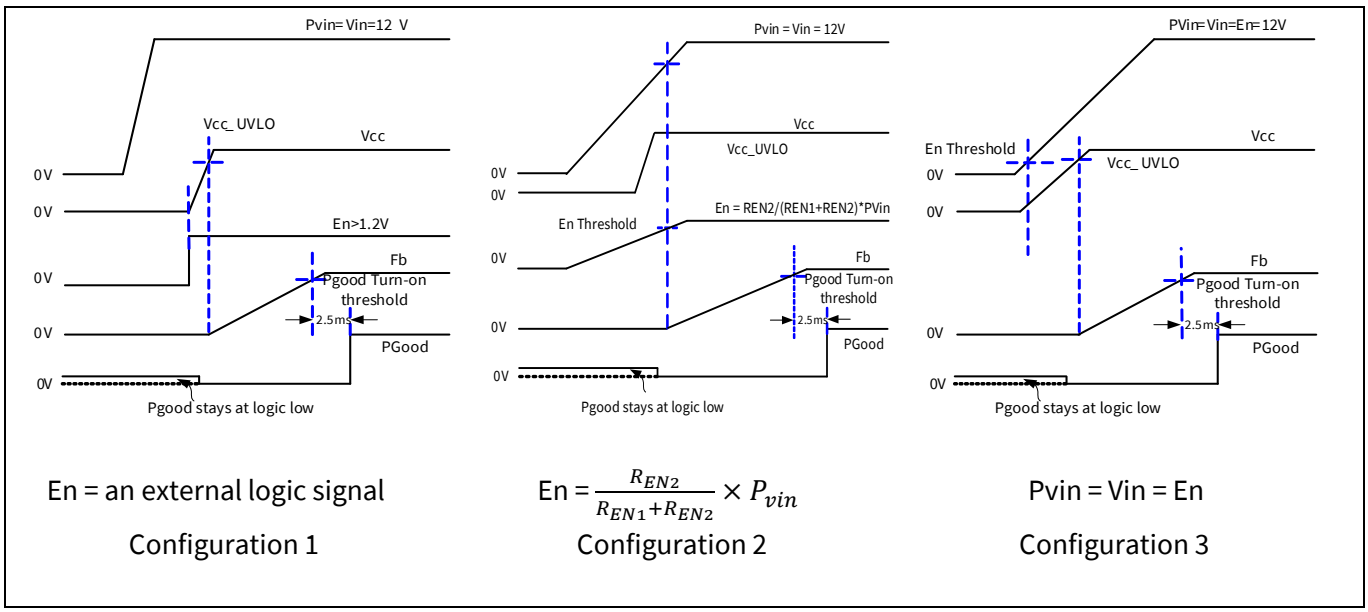


Figure 7 Enable Configurations



En = an external logic signal

Configuration 1

$En = \frac{R_{EN2}}{R_{EN1}+R_{EN2}} \times P_{vin}$

Configuration 2

Pvin = Vin = En

Configuration 3

Figure 8 Start-up sequence

12.3 FCCM and DEM Operation

The IR3899A offers two operation modes: Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DEM). With FCCM, the IR3899A always operates as a synchronous buck converter with a pseudo-constant switching frequency leading to small output voltage ripple. In DEM, the synchronous FET is turned off when the inductor current is close to zero, reducing the switching frequency and improving efficiency at light load. At heavy load, both FCCM and DEM operate in the same way. The operating mode can be selected with the TON/MODE pin, as shown in **Table 2**. It should be noted that the selection of the operating mode cannot be changed on the fly. To load a new TON/MODE configuration, EN or VCC voltage must be cycled.

12.4 Pseudo-Constant Switching Frequency

The IR3899A offers eight programmable switching frequencies, f_{sw}, from 600 kHz to 2 MHz, by connecting an external resistor from the TON/MODE pin to ground. Based on the selected f_{sw}, the IR3899A generates the corresponding on-time of the Control FET for a given PV_{in} and V_o, as shown by the formula below.

$$T_{on} = \frac{V_0}{PV_{in}} \times \frac{1}{f_{sw}}$$

Where f_{sw} is the desired switching frequency. During operation, the IR3899A monitors PV_{in} and V_o, and can automatically adjust the on-time to maintain the pre-selected f_{sw}. As load current increases, the switching frequency can increase to compensate for power losses.

Table 2 lists resistor values for the TON/MODE pin. In this table, E96 resistors with ±1% tolerance are used. To load a new TON/MODE configuration, En or VCC voltage must be cycled.

Table 2 Configuration Resistors for TON/MODE Pin

TON/MODE Resistor (kΩ) ±1% Tolerance	Freq (kHz)	Mode
0	600	FCCM
1.5	800	
2.49	1000	
3.48	1200	
4.53	1400	
5.76	1600	
7.32	1800	
8.87	2000	
10.5	600	DEM
12.1	800	
14	1000	
16.2	1200	
18.7	1400	
21.5	1600	
24.9	1800	
28.7	2000	
TON/MODE = Floating	800	FCCM

12.5 Soft-start

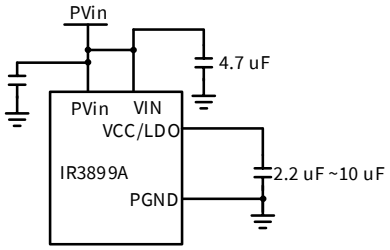
The IR3899A has an internal digital soft-start to control the output voltage rise and to limit the current surge at start-up. To ensure a correct start-up, the soft-start sequence initiates when the En and VCC voltages rise above their respective thresholds. The internal soft-start signal linearly rises from 0 V to 0.6 V in a defined time duration. The soft-start time does not change with the output voltage. During soft-start, the IR3899A operates in DEM until 1 ms after the output voltage ramps above the PGood turn-on threshold. The IR3899A has a fixed soft-start time of 2 ms.

12.6 Pre-bias Start-up

The IR3899A is able to start up into a pre-charged output without causing oscillations and disturbances of the output voltage. When the IR3899A starts up with a pre-biased output voltage, both control FET and Sync FET are kept off until the internal soft-start signal exceeds the FB voltage.

12.7 Internal Low - Dropout (LDO) Regulator

The IR3899A has an integrated low-dropout LDO regulator providing the bias voltage for the internal circuitry. To minimize standby current, the internal LDO is disabled when the EN voltage is pulled low. The Vin pin is the input of the LDO. The IR3899A supports internal LDO with single rail operation, i.e., the Vin pin should always be connected to the PVin pin. **Figure 9** illustrates the configuration of VCC/LDO, and the Vin pin.



Single rail operation with the internal LDO

Figure 9 Configuration of using the internal LDO.

Section **7.1** specified the recommended operating voltage range of PVin. The following design guidelines are recommended when configuring the VCC/LDO.

- Place a bypass capacitor to minimize disturbances on the VCC pin. For single rail operation using the internal LDO, a 4.7 µF low ESR ceramic capacitor must be used between Vin pin and PGND and a low ESR ceramic capacitor with value between 2.2 µF and 10 µF is required to be placed close to the VCC/LDO with reference to PGND. 10 µF MLCC is recommended for the VCC bypass capacitor when VIN is below 5.5 V.
- For applications using the internal LDO with 4.3 V ≤ VIN ≤ 5.4 V, the LDO can be in the dropout mode. It is important to ensure that the LDO voltage does not fall below the VCC UVLO threshold voltage. At Vin = 4.3 V, I_{CC} must not exceed 50 mA under all operating conditions such as during a step-up load transient, in which the control loop may require the increase of f_{sw}. OCP limits can also be reduced due to the lower VCC voltage.

12.8 Over Current Protection (OCP)

The IR3899A offers cycle-by-cycle OCP response with two selectable current limits set by floating the ILIM pin or shorting it to GND. The selected OCP limit is loaded to the IC during power up and cannot be changed on the fly. To change the OCP limit, users must cycle the En signal or VCC voltage. Cycle-by-cycle OCP response allows the IR3899A to fulfill a brief high current demand, such as a high inrush current during start-up. Detailed operation is explained as follows:

OCP is activated when En voltage is above its threshold. The OCP circuitry monitors the current of the Synchronous MOSFET through its $R_{DS\,(on)}$. When a new PWM pulse is requested by the control loop, if the current of the Synchronous MOSFET exceeds the OCP limit, the IR3899A skips the PWM pulse and extends the on-time of the Synchronous MOSFET until the current drops below the OCP limit. OCP operation is also illustrated in **Figure 10**. During OCP events, the valley of the inductor current is regulated around the OCP limit. However, during the first switching cycle when the OCP is tripped, the valley of the inductor current can drop slightly below the OCP limit. It should be noted that OCP events do not pull the PGood signal low unless the V_o drops below the PGood turn-off threshold. If the OCP event persists, the output voltage can eventually drop below the Under Voltage Protection (UVP) threshold and trigger UVP. Then the IR3899A enters hiccup mode.

The OCP limits are thermally compensated. The OCP limits specified in Section **7.2** refer to the valley of the inductor current when OCP is tripped. Therefore, the corresponding output DC current can be calculated as follows:

$$I_{out\_OCP} = I_{LIM} + \frac{\Delta i_L}{2}$$

Where: I_{out_OCP} = Output DC current when OCP is tripped. I_{LIM} = OCP limit specified in the Section **7.2**, which is the valley of inductor current. ΔiL = Peak-peak inductor ripple current.

To avoid inductor saturation during OCP events, the following criterion is recommended for the inductor saturation current rating.

$$I_{sat} \geq I_{LIM\_max} + \Delta i_L$$

Where: I_{sat} is the inductor saturation current and I_{LIM_max} is the maximum spec of the OCP limit.

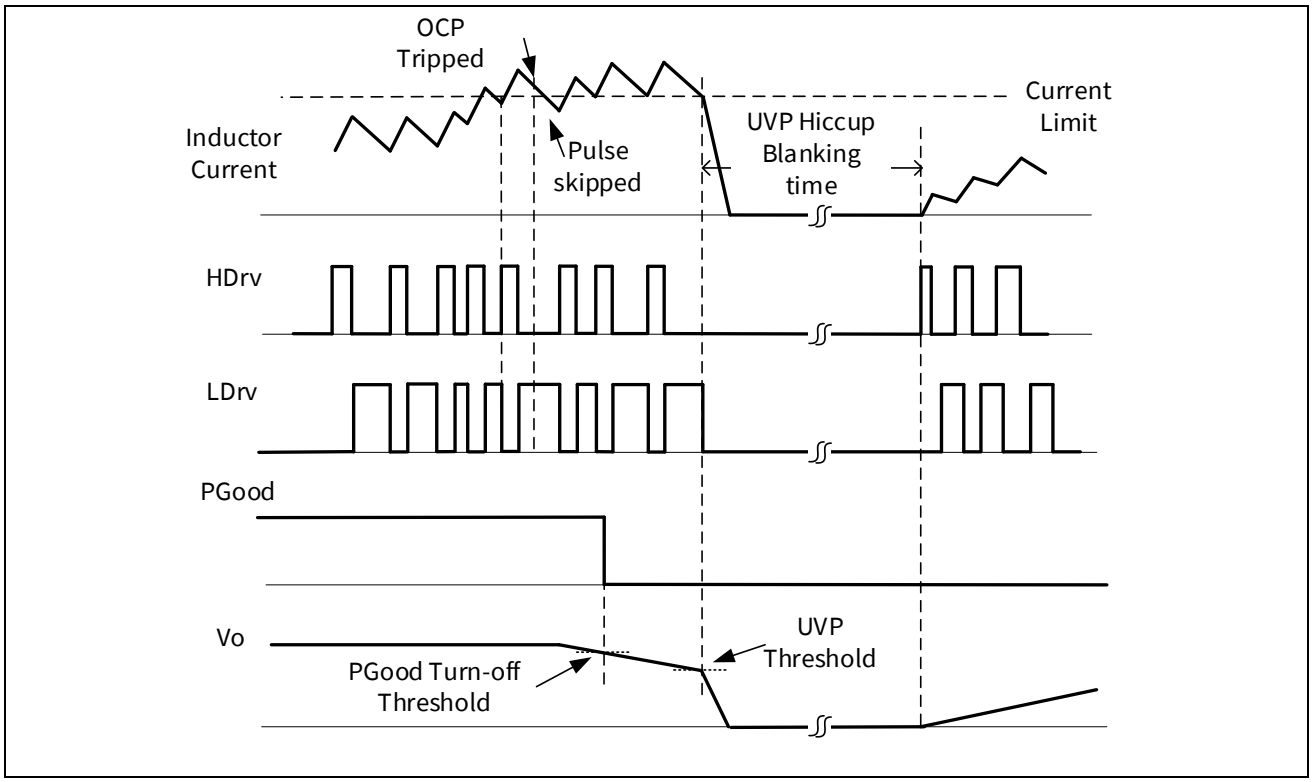


Figure 10 Cycle-by-cycle OCP response

12.9 Under Voltage Protection (UVP)

Under Voltage Protection (UVP) provides additional protection during OCP fault or other faults. UVP protection is enabled when the soft-start voltage rises above 100 mV. UVP circuitry monitors VSNS voltage. When VSNS is below the UVP threshold for 5 µs (typical), an under voltage trip signal asserts and both Control MOSFET and Synchronous MOSFET are turned off. The IR3899A enters hiccup mode with a blanking time of 20 ms, during which Control MOSFET and Synchronous MOSFET remain off. After the completion of blanking time, the IR3899A attempts to recover to the nominal output voltage with a soft-start, as shown in **Figure 10**. The IR3899A will repeat hiccup mode and attempt to recover until the UVP condition is removed.

12.10 Over Voltage Protection (OVP)

Over Voltage Protection (OVP) is achieved by comparing the VSNS voltage to an OVP threshold voltage. When the VSNS voltage exceeds the OVP threshold, an over voltage trip signal asserts after 4 µs (typical) delay. The Control MOSFET is latched off immediately and Pgood flags low. The Synchronous MOSFET remains on to discharge the output capacitor. When VSNS voltage drops below around 115% of the reference voltage, Synchronous MOSFET turns off to prevent complete depletion of the output capacitors. **Figure 11** illustrates the OVP operation. The OVP comparator becomes active when the En signal is above the start threshold.

IR3899A has a Latched OVP response, i.e., when OVP is triggered, the Control FET remains latched off until either VCC voltage or En signal is cycled.

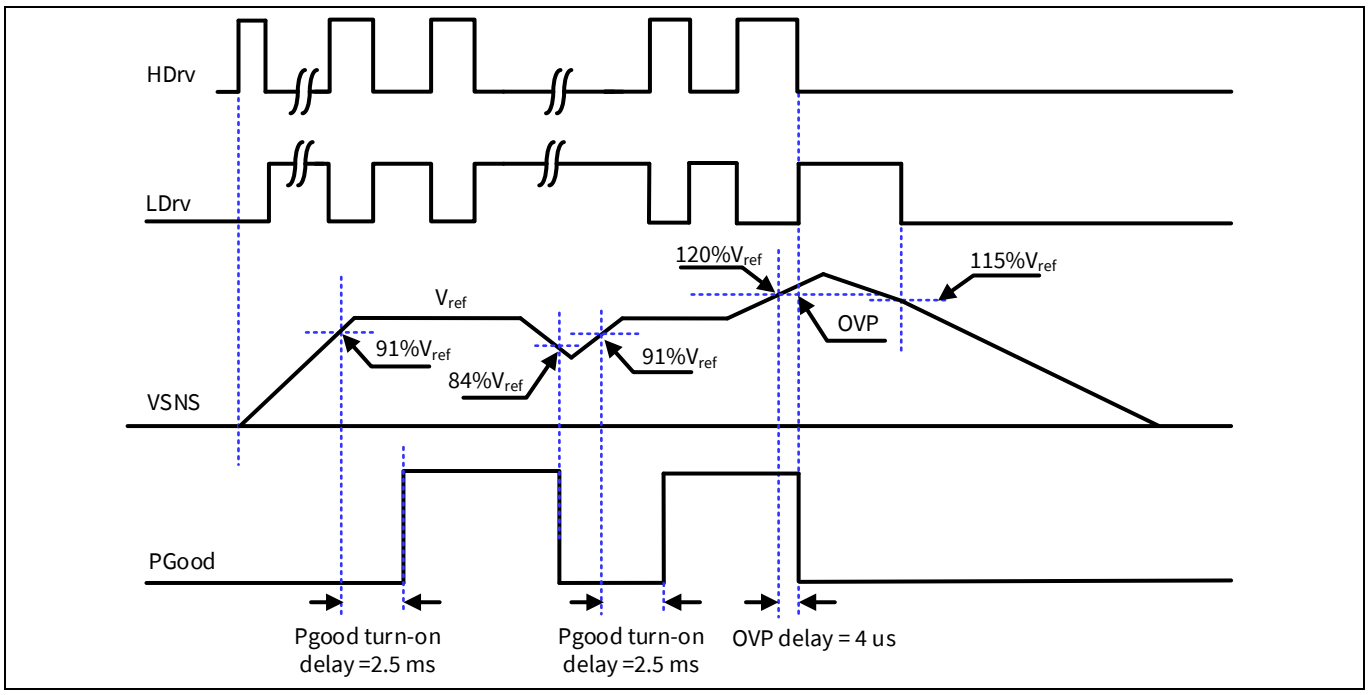


Figure 11 Over voltage protection response and Pgood behavior.

12.11 Over Temperature Protection (OTP)

Temperature of the controller is monitored internally. When the temperature exceeds the over temperature threshold, OTP circuitry turns off both Control and Synchronous MOSFETs and resets the internal soft start. Automatic restart is initiated when the sensed temperature drops back into the operating range. The thermal shutdown threshold has a hysteresis of 20 °C.

12.12 Power Good (Pgood) Output

The Pgood pin is the open drain of an internal NFET, and must be externally pulled high through a pull-up resistor. The Pgood signal is high when three criteria are satisfied:

1. En signal and VCC voltage are above their respective thresholds.

2. No over voltage or over temperature faults occur.

3. V_o is within regulation.

In order to detect if V_O is in regulation, the Pgood comparator continuously monitors VSNS voltage. When VSNS voltage ramps up above the upper threshold, the Pgood signal is pulled high after 2.5 ms. When VSNS voltage drops below the lower threshold, the Pgood signal is pulled low immediately. **Figure 11** illustrates the Pgood response.

During start-up with a pre-biased output voltage, the Pgood signal is held low before the first PWM is generated and is then pulled high with 2.5 ms delay after VSNS voltage rises above the Pgood threshold. IR3899A also integrates an additional PFET in parallel to the Pgood NFET, as shown in **Figure 2**. This PFET allows the Pgood signal to stay at logic low when the VCC voltage is not present and the Pgood pin is pulled up by an external bias voltage. Please refer to **Figure 8**. Since the Pgood PFET has relatively higher on resistance, a 50 kΩ pull-up resistor is needed for a Pgood bias voltage of 3.3V to maintain the Pgood signal at logic low when Pgood PFET is on.

12.13 Minimum ON – Time and Minimum OFF – Time

The minimum on-time refers to the shortest time for the Control MOSFET to be reliably turned on. The minimum off-time refers to the minimum time duration in which the Synchronous FET stays on before a new PWM pulse is generated. The minimum off-time is needed for IR3899A to charge the bootstrap capacitor, and to sense the current of the Synchronous MOSFET for OCP.

For applications requiring a small duty cycle, it is important that the selected switching frequency results in an on-time larger than the maximum spec of the minimum on-time in Section **7.2**. Otherwise, the resulting switching frequency may be lower than the desired target. The following formula should be used to check for the minimum on-time requirement.

$$\frac{V_0}{kf_{sw} \times V_{in}} > \max\ spec\ of\ T_{on(\min)}$$

Where f_{sw} is the desired switching frequency. *K* is the variation of the switching frequency. As a rule of thumb, select *k* = 1.25 to ensure design margin.

For applications requiring a high duty cycle, it is important to make sure a proper switching frequency is selected so that the resulting off-time is longer than the maximum spec of the minimum off-time in Section **7.2**, which can be calculated as shown below.

$$\frac{V_{in} - V_0}{kf_{sw} \times V_{in}} > \max\ spec\ of\ T_{off(\min)}$$

Where f_{sw} is the desired switching frequency. *K* is the variation of the switching frequency. As a rule of thumb, select *k* = 1.25 to ensure design margin.

The resulting maximum duty cycle is therefore determined by the selected on-time and minimum off-time.

$$D_{max} = \frac{T_{on}}{T_{on} + T_{off(\min)}}$$

12.14 Selection of Feedforward Capacitor and Feedback Resistors

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.6 V. The divider ratio is set to provide 0.6 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

$$V_O = V_{ref} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Where R_{FB1} and R_{FB2} are the top and bottom feedback resistors.

A small MLCC capacitor, C_{ff}, is preferred in parallel with the top feedback resistor, R_{FB1}, to provide extra phase boost and improve the transient load response, as shown in **Figure 12.** The following formula can be used to help select C_{ff} and R_{FB1}. The value of C_{ff} is recommended to be 100 pF or higher to minimize the impact of circuit parasitic capacitance, where L_O and C_O are the output LC filter of the buck regulator. Table 3 lists the suggested 'm' for some common outputs. C_{ff} and R_{FB1} may be further optimized based on the transient load tests.

$$R_{FB1}C_{ff} = \frac{\sqrt{L_0C_0}}{m \times 4.9}$$

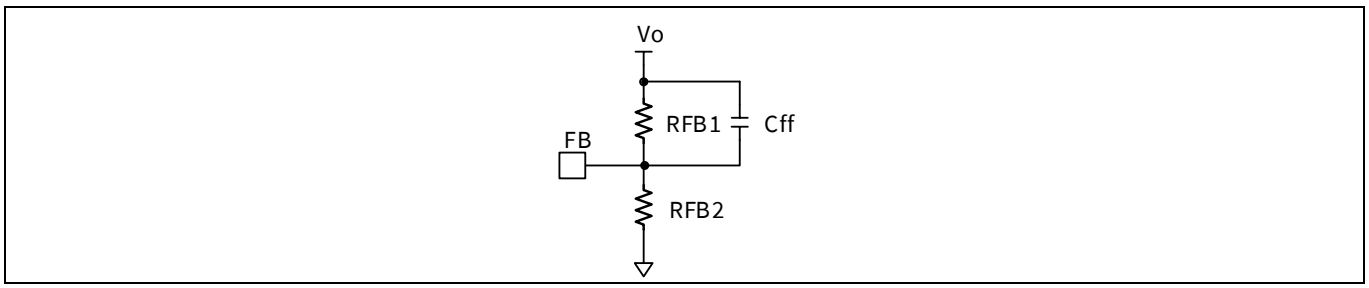


Figure 12 Configuration of feedforward capacitor, Cff.

Table 3 Selection of m

Vo	m
3.0 V ≤ Vo ≤ 5.0 V	0.3
1.2 V < Vo < 3.0 V	0.5
Vo ≤ 1.2 V	0.7

12.15 Resistors for Configuration Pins

To properly configure the TON/ MODE pin, E96 resistors with ±1% tolerance must be used per **Table 2** and Section **7.2**. If E12 resistor values are preferred, the E96 resistors can be replaced with two or three E12 resistors in series, as shown in Table 4. Note that the tolerance of E12 resistors must be ±0.1%.

Table 4 Replacement of E96 configuration resistors with E12 resistors in series

E96 ±1%	E12 ±0.1% ($R = R_{S1} + R_{S2}$ or $R_{S1} + R_{S2} + R_{S3}$)		
R (kΩ)	R_{S1} (kΩ)	R_{S2} (kΩ)	R_{S3} (kΩ)
4.53	2.7	1.8	N/A
1.50	1.5	0	N/A
5.76	5.6	0.15	N/A
2.49	1.8	0.68	N/A
7.32	6.8	0.56	N/A
3.45	3.3	0.15	N/A
8.87	8.2	0.68	N/A
10.5	10	0.47	N/A
12.1	12	0.1	N/A
21.5	18	3.3	N/A
14	10	3.9	N/A
24.9	22	2.7	N/A
16.2	15	1.2	N/A
28.7	27	1.8	N/A
21.5	18	3.3	0.18
24.9	22	2.7	0.18

13 Design example

In this section, an example is used to demonstrate how to design a buck regulator with the IR3899A. The application circuit is shown in **Figure 13**. The design specifications are given below:

- PV_{in} = 12 V (±10%)
- V_O = 1.2 V
- I_O = 9 A
- V_O ripple voltage = ± 1% of V_O
- Load transient response = ± 3% of V_O with a step load current = 4.5 A and slew rate = 5 A/µs

13.1 Enabling the IR3899A

The IR3899A has a precise Enable threshold voltage, which can be used to implement a UVLO of the input bus voltage by connecting the En pin to Pvin with a resistor divider, as shown in Configuration 2 of **Figure 7**. The Enable feedback resistor, R_{EN1} and R_{EN2}, can be calculated as follows.

$$PV_{in(\min)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq V_{EN(\max)}$$

$$R_{EN2} \geq R_{EN1} \times \frac{V_{EN(\max)}}{PV_{in(\min)} - V_{EN(\max)}}$$

Where $V_{EN\ (max)}$ is the maximum spec of the Enable-start-threshold as defined in Section **7.2**. For $Pvin_{\ (min)}$ =10.8 V, select R_{EN1} = 49.9 kΩ and R_{EN2} = 7.5 kΩ.

13.2 Programming the Switching Frequency and Operation Mode

The IR3899A has very good efficiency performance and is suitable for high switching frequency operation. In this case, 600 kHz is selected to achieve a good compromise between efficiency, passive component size and dynamic response. In addition, FCCM operation is selected to ensure a small output ripple voltage over the entire load range. To select 600 kHz and FCCM operation, the TON/MODE pin is connected to a 0 kΩ resistor to GND per **Table 2**.

13.3 Selecting Input Capacitors

Without input capacitors, the pulse current of the Control MOSFET is provided directly from the input supply. Due to the impedance of the cable, the pulse current can cause disturbance on the input voltage and potential EMI issues. The input capacitors filter the pulse current, resulting in almost constant current from the input supply. The input capacitors should be selected to tolerate the input pulse current, and to reduce the input voltage ripple. The RMS value of the input ripple current can be expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)}$$

$$D = \frac{V_o}{PV_{in}}$$

Where I_{RMS} is the RMS value of the input capacitor current. I_o is the output current and D is the Duty Cycle. For I_o = 9 A and $D_{(max)}$ = 0.1, the resulting RMS current flowing into the input capacitor is I_{rms} = 2.7 A.

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated as follows.

$$C_{in(\min)} > \frac{I_o \times (1-D) \times D}{f_{sw} \times (\Delta PV_{in} - ESR \times I_o \times (1-D))}$$

Where ΔPvin is the maximum allowable peak-to-peak input ripple voltage, and ESR is the equivalent series resistance of the input capacitors. Ceramic capacitors are recommended due to low ESR, ESL and high RMS current capability. For I_o = 9 A, f_{sw} = 600 kHz, ESR = 3 mΩ, and ΔPvin = 240 mV, $C_{in(min)}$ > 11.0 µF. To account for the derating of ceramic capacitors under a bias voltage, four 22 µF/0805/25V MLCC are used for the input capacitor. In addition, a bulk capacitor is recommended if the input supply is not located close to the voltage regulator.

13.4 Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency and high output noise, but helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor (Δi) is found between 20% and 50% of the output current.

The inductor saturation current must be higher than the maximum spec of the OCP limit plus the peak-to-peak inductor ripple current. For some core material, inductor saturation current may decrease with increasing temperature. It is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relations:

$$L = (PV_{in(\max)} - V_o) \times \frac{D_{min}}{\Delta i_{L(\max)} \times F_{sw}}$$

$$D_{min} = \frac{V_o}{PV_{in(\max)}}$$

$$I_{sat} \geq OCP_{max} + \Delta i_{L(\max)}$$

Where: $PV_{in\ (max)}$ = Maximum input voltage; ΔiL_{max} = Maximum peak-to-peak inductor ripple current; OCP_{max} = maximum spec of the OCP limit as defined in Section **7.2**; and I_{sat} = inductor saturation current. In this case, select inductor L = 470 nH to achieve ΔiL_{max} = 43% of I_{omax}. The I_{sat} should be no less than 19.0 A.

13.5 Output Capacitor Selection

The output capacitor selection is mainly determined by the output voltage ripple and transient requirements.

To satisfy the V_o ripple requirement, C_o should satisfy the following criterion:

$$C_o > \frac{\Delta i_{Lmax}}{8 \times \Delta V_{or} \times f_{sw}}$$

Where ΔV_{or} is the desired peak-to-peak output ripple voltage. For ΔiL_{max} = 3.8 A, ΔV_{or} = 24 mV, f_{sw} = 600 kHz, C_o must be larger than 33 µF. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. It is suggested to use Multi-Layer Ceramic Capacitor (MLCC) for their low ESR, ESL and small size.

To meet the transient response requirements, the output capacitors should also meet the following criterion:

$$C_o > \frac{L \times \Delta I_{o(\max)}^2}{2 \times \Delta V_{oL} \times V_o}$$

Where ΔV_{OL} is the allowable V_o deviation during the load transient. $\Delta I_{o(max)}$ is the maximum step load current. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not

considered in the calculation shown above. Extra capacitance is usually needed to meet the transient requirements. As a rule of thumb, we can triple the C_o that is calculated above as a starting point, and then optimize the design based on bench measurement. In this case, to meet the transient load requirement (i.e. ΔV_{OL}= 54 mV, $\Delta I_{o(max)}$ = 4.5 A), select C_o = ~110 µF. For more accurate estimation of C_o, simulation tools should be used to aid the design.

13.6 Output Voltage Programming

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.6 V. The divider ratio is set to provide 0.6 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

$$V_o = V_{ref} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

Where R_{FB1} and R_{FB2} are the top and bottom feedback resistors. Select R_{FB1} = 10 kΩ and R_{FB2} = 10 kΩ, to achieve V_o = 1.2 V. The same resistor divider can be used at the VSNS pin to achieve the same voltage scaling factor.

13.7 Feedforward Capacitor

A small MLCC capacitor, C_{ff}, can be placed in parallel with the top feedback resistor, R_{FB1}, to improve the transient response. Based on Section **12.14**, C_{ff} can be selected using the following formula.

$$R_{FB1}C_{ff} = \frac{\sqrt{L_0 C_0}}{0.7 \times 4.9}$$

With Lo = 470 nH, Co = 114 µF and R_{FB1} = 10 kΩ, C_{ff} = ~220 pF. C_{ff} can be further optimized based on bench testing of transient load response.

13.8 Bootstrap Capacitor

For most applications, a 0.1 µF ceramic capacitor is recommended for bootstrap capacitor placed between SW and BOOT. For applications requiring Pvin equal to or above 14 V, a small resistor between 1 Ω and 2 Ω can be used in series with the BOOT pin to ensure the maximum SW node spike voltage does not exceed 20 V.

13.9 Vin and VCC/LDO bypass Capacitor

Please see the recommendation in **Section 12.7**. A 10 µF MLCC is selected for the VCC/LDO bypass capacitor and a 4.7 µF MLCC is selected for the Vin bypass capacitor.

14 Application information

14.1 Application Diagram

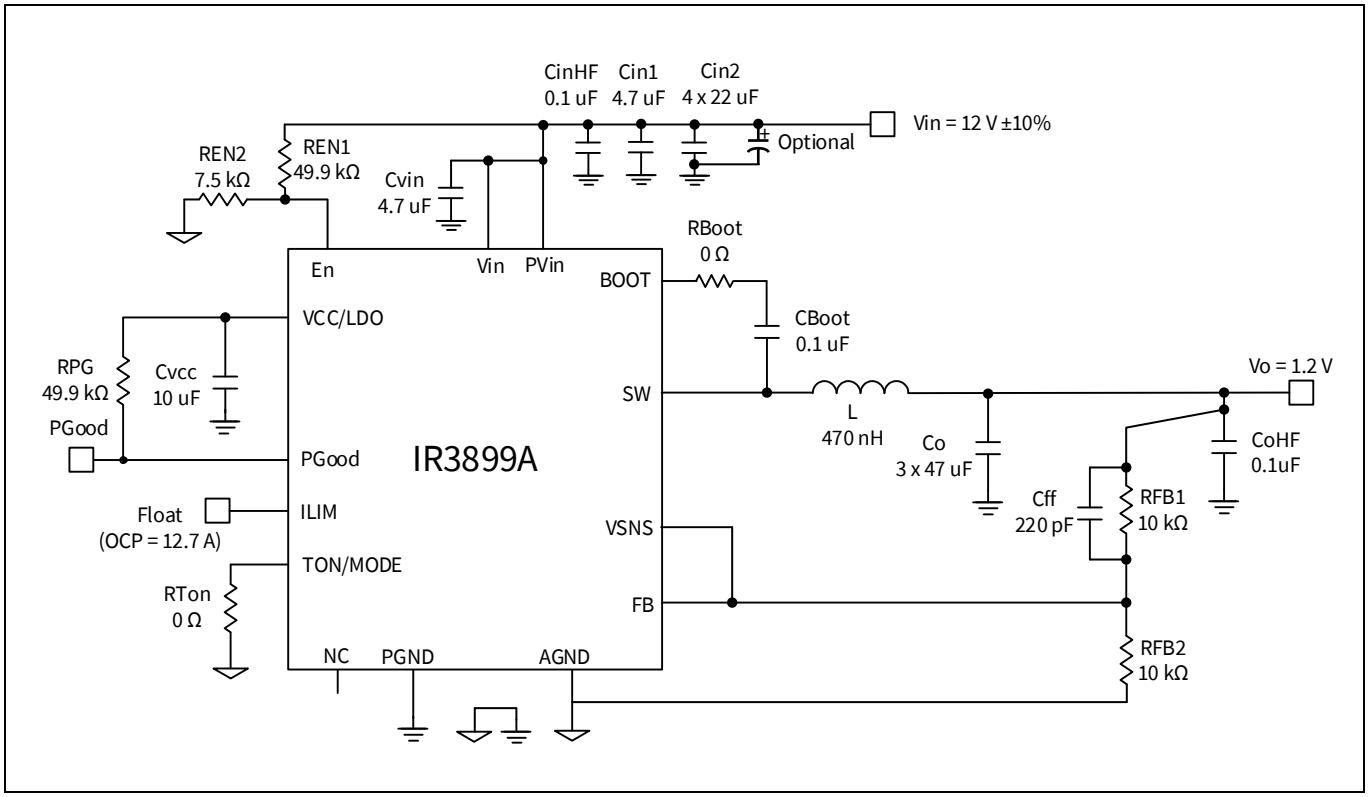


Figure 13 Application diagram of IR3899A. Pvin = 12 V, Vo = 1.2 V, Io = 9 A, fsw = 600 kHz.

14.2 Typical Operating Waveforms

PV_{in} = V_{in} = 12.0 V, Vo = 1.2 V, I_o = 0 – 9 A, f_{sw} = 600 kHz, Room Temperature, no airflow

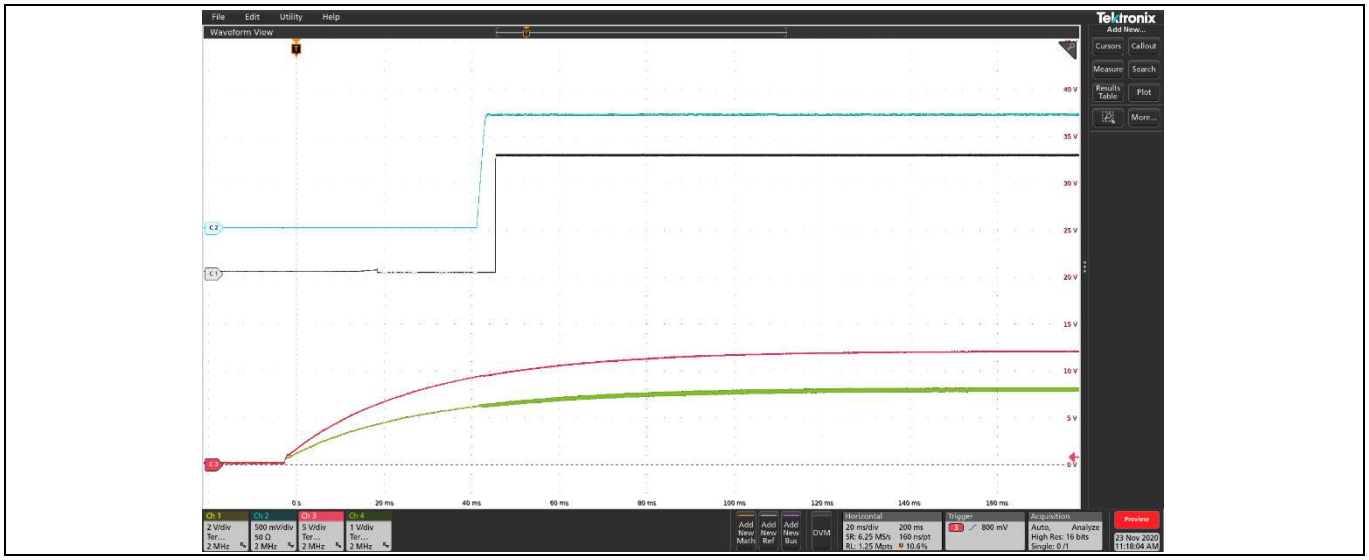


Figure 14 Start up at 9 A Load, (Ch1: Pgood, Ch2: Vout, Ch3: Pvin, Ch4: Enable)

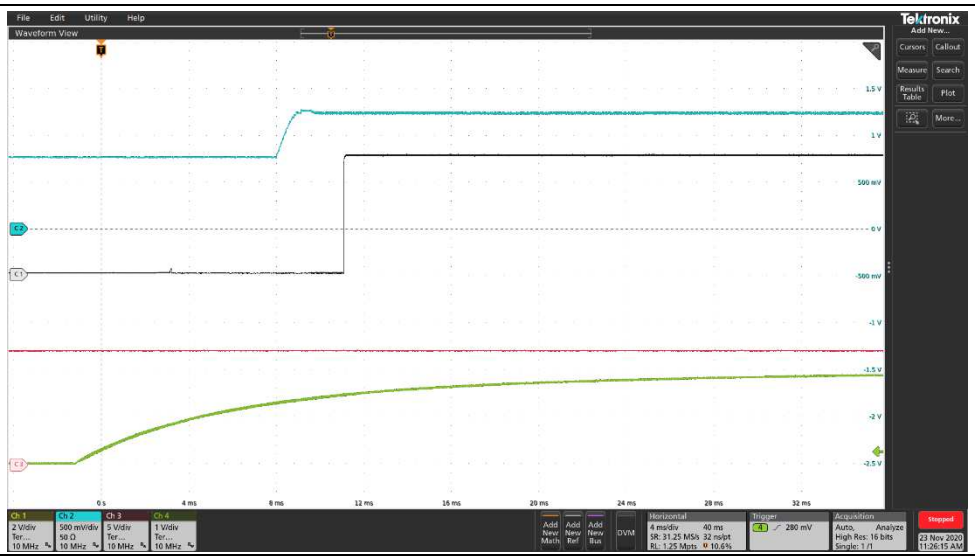


Figure 15 Pre-bias Start up at 0 A Load, (Ch1: Pgood, Ch2: Vout, Ch3: Pvin, Ch4: Enable)

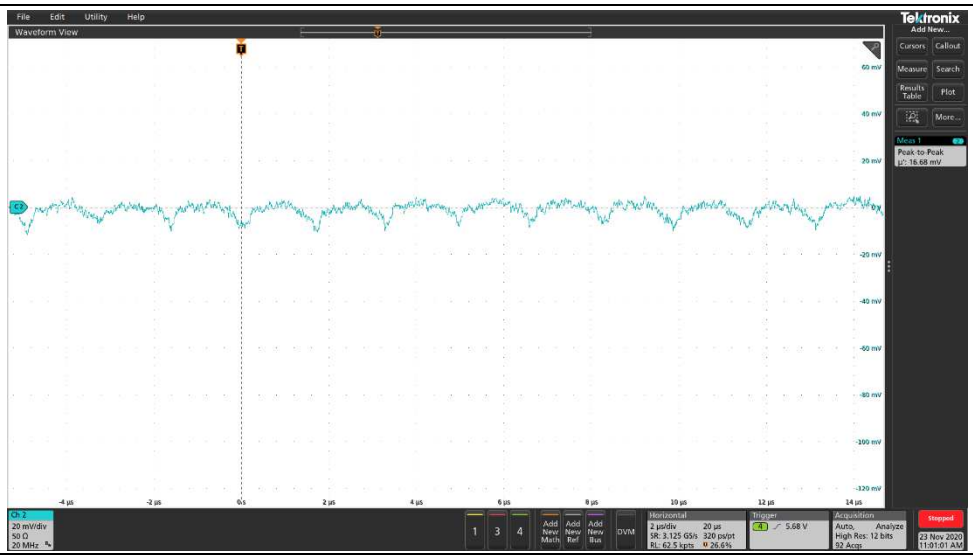


Figure 16 Vout ripple at 9 A Load, fsw = 600 kHz, (Ch2: Vo)

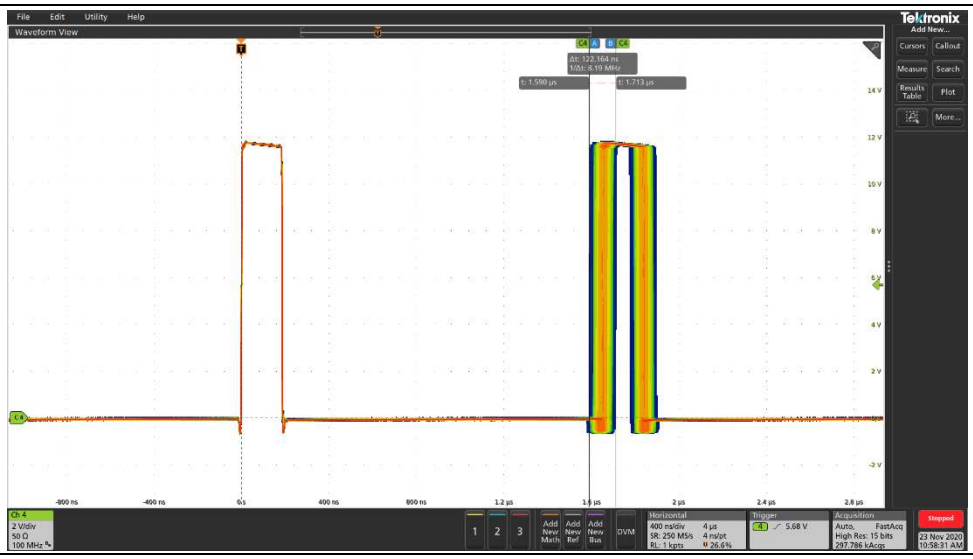


Figure 17 SW node, 9 A load, fsw = 600 kHz, (Ch4: SW)

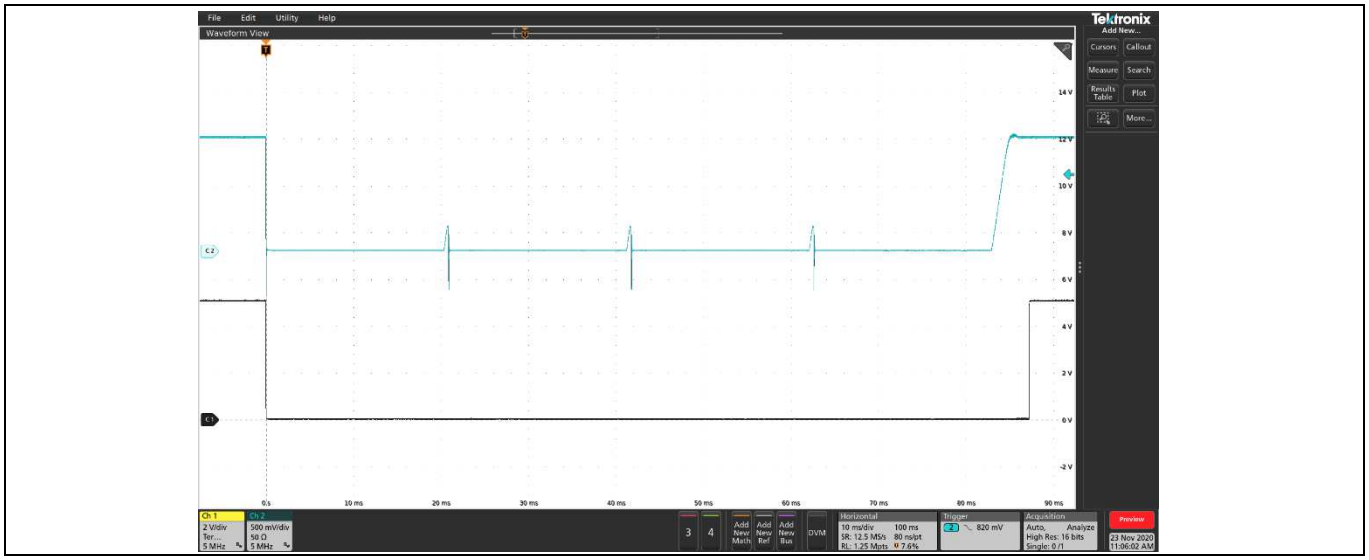


Figure 18 Short circuit and UVP (Hiccup), (Ch1: Pgood, Ch2: Vo)

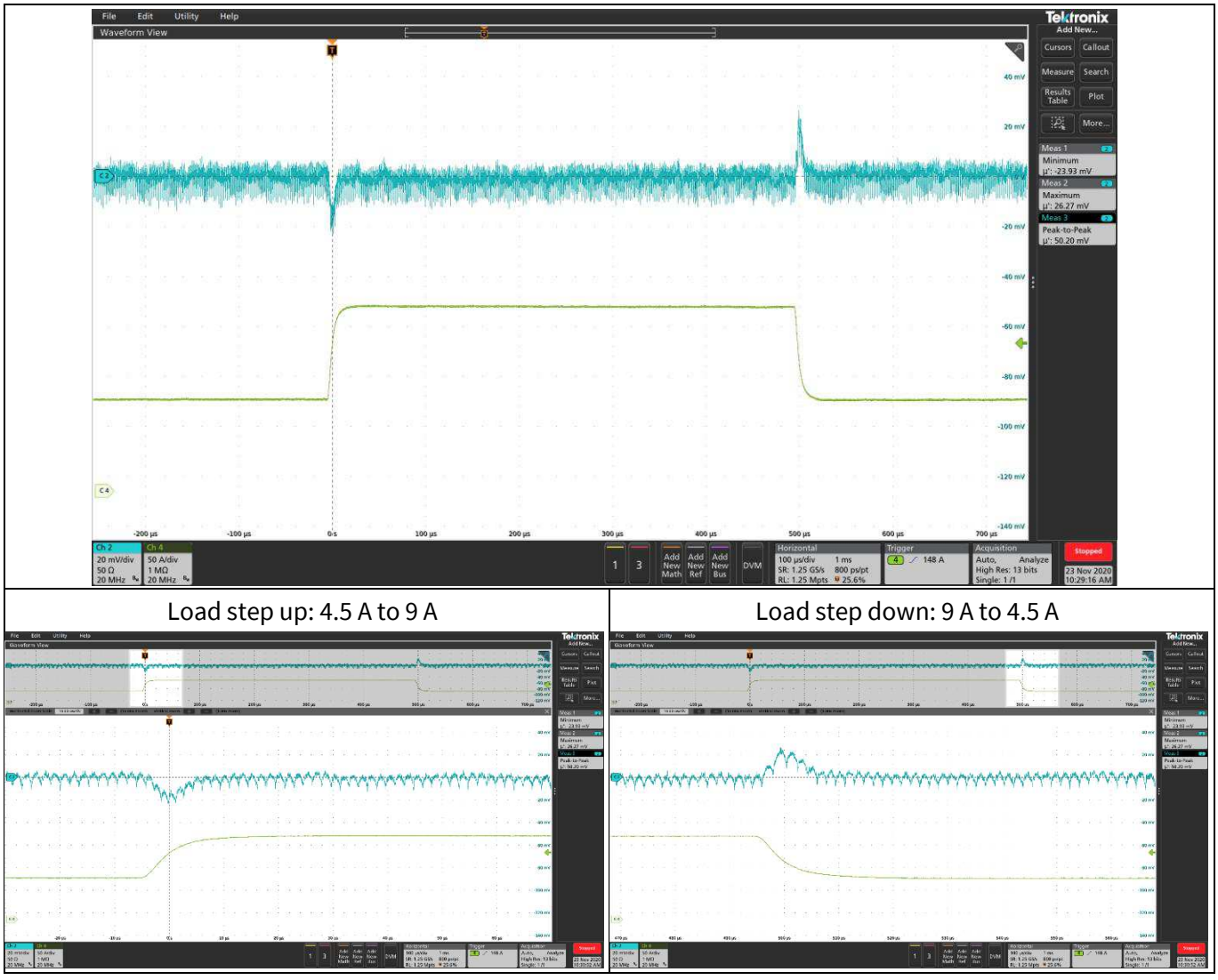


Figure 19 Transient response at 4.5 A step load current: Io= 4.5 A – 9 A, (Ch2: Vo, Ch4: Io), pk-pk: 50.2 mV, fsw = 600 kHz

15 Layout Recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results. The following design guidelines are recommended to achieve the best performance.

- Bypass capacitors, including input/output capacitors, Vin and VCC bypass capacitors, should be placed as close to the corresponding pins as possible.
- Place bypass capacitors from IR3899A power input (Drain of Control MOSFET) to PGND (Source of Synchronous MOSFET) to reduce noise and ringing in the system. The output capacitors should be terminated to a ground plane that is away from the input PGND to mitigate switching spikes on the Vout. The Vin and VCC bypass capacitors should be terminated to PGND.
- Place a boot strap capacitor as close as possible to IR3899A BOOT and SW pins to minimize loop inductance.
- SW node copper should only be routed on the top layer to minimize the impact of switching noise.
- Connect the AGND pin to the PGND pad through a single point connection. On the IR3899A demo board, AGND pin is connected to the exposed AGND pad (Pin 4) and then connected to the internal PGND layer through thermal via holes.
- Via holes can be placed on Pvin and PGND pads to aid thermal dissipation.
- Wide copper polygons are desired for Pvin and PGND connections in favor of power loss reduction and thermal dissipation. Sufficient via holes should be used to connect power traces between different layers.
- To implement the V_o sensing, the following design guidelines should be followed, as illustrated in **Figure 13**.
    - The output voltage can be sensed from a high-frequency bypass capacitor of 0.1 µF or higher, through a 15 mil PCB trace.
    - Keep the Vout sense line away from any noise sources and shield the sense line with ground planes.
    - The sense trace is connected to a feedback resistor divider with the lower resistor terminated at the AGND pin.

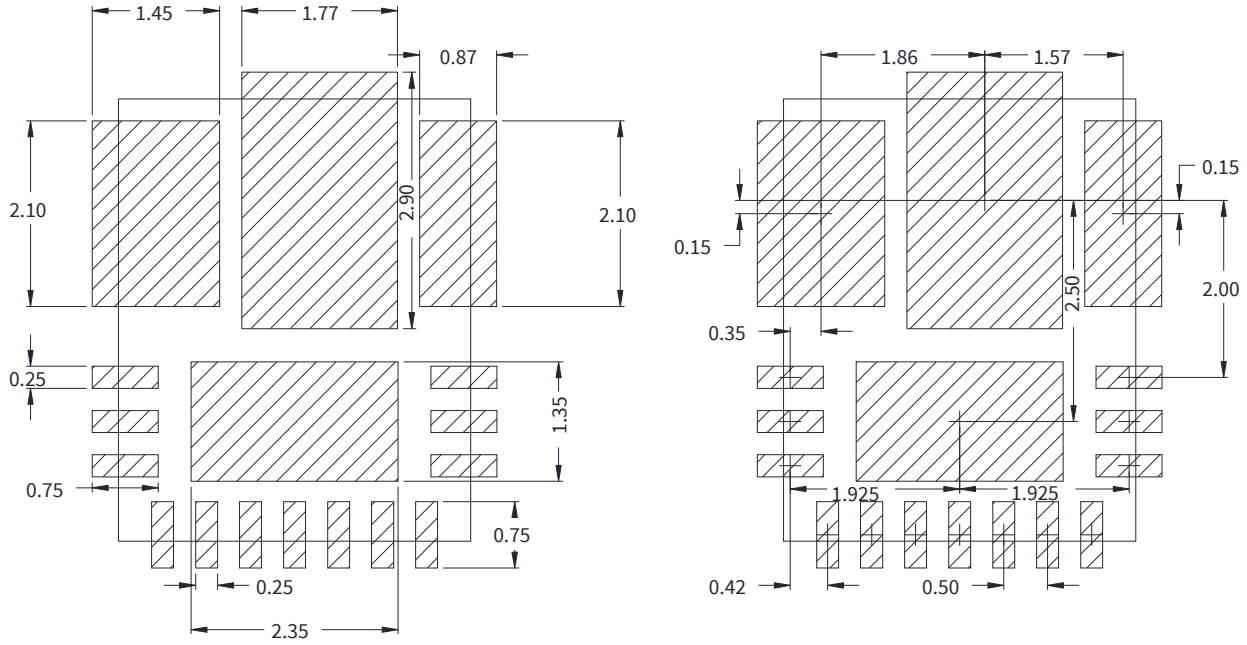
The EN pin and configuration pins including TON/MODE and ILIM should be terminated to a quiet ground. On the IR3899A standard demo board, they are terminated to the PGND copper plane away from the power current flow. Alternatively, they can be terminated to a dedicated AGND PCB trace.

15.1 Solder mask

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD). This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the openings in the solder mask. This allows for layers to be misaligned by up to 0.1 mm on both axes. Ensure that the solder resist between the smaller signal lead areas is at least 0.15 mm wide due to the high x/y aspect ratio of the solder mask strip.

PCB PAD



SOLDER MASK DESIGN

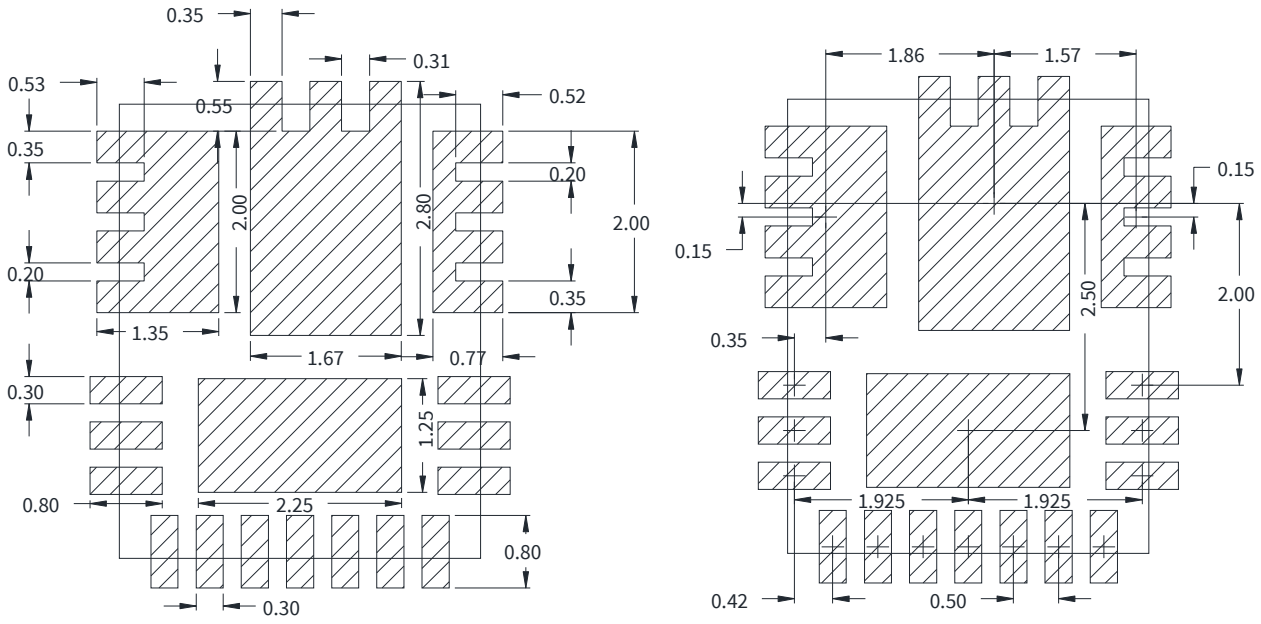


Figure 20 PCB Metal and Solder mask (all dimensions in mm)

15.2 Stencil design

Stencils for PQFN packages can be used with thicknesses of 0.100-0.250 mm (0.004-0.010”). Stencils thinner than 0.100 mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125 mm-0.200 mm (0.005-0.008”), with suitable reductions, give the best results. A recommended stencil design is shown below. This design is for a stencil thickness of 0.127 mm (0.005”). The reduction should be adjusted for stencils of other thicknesses.

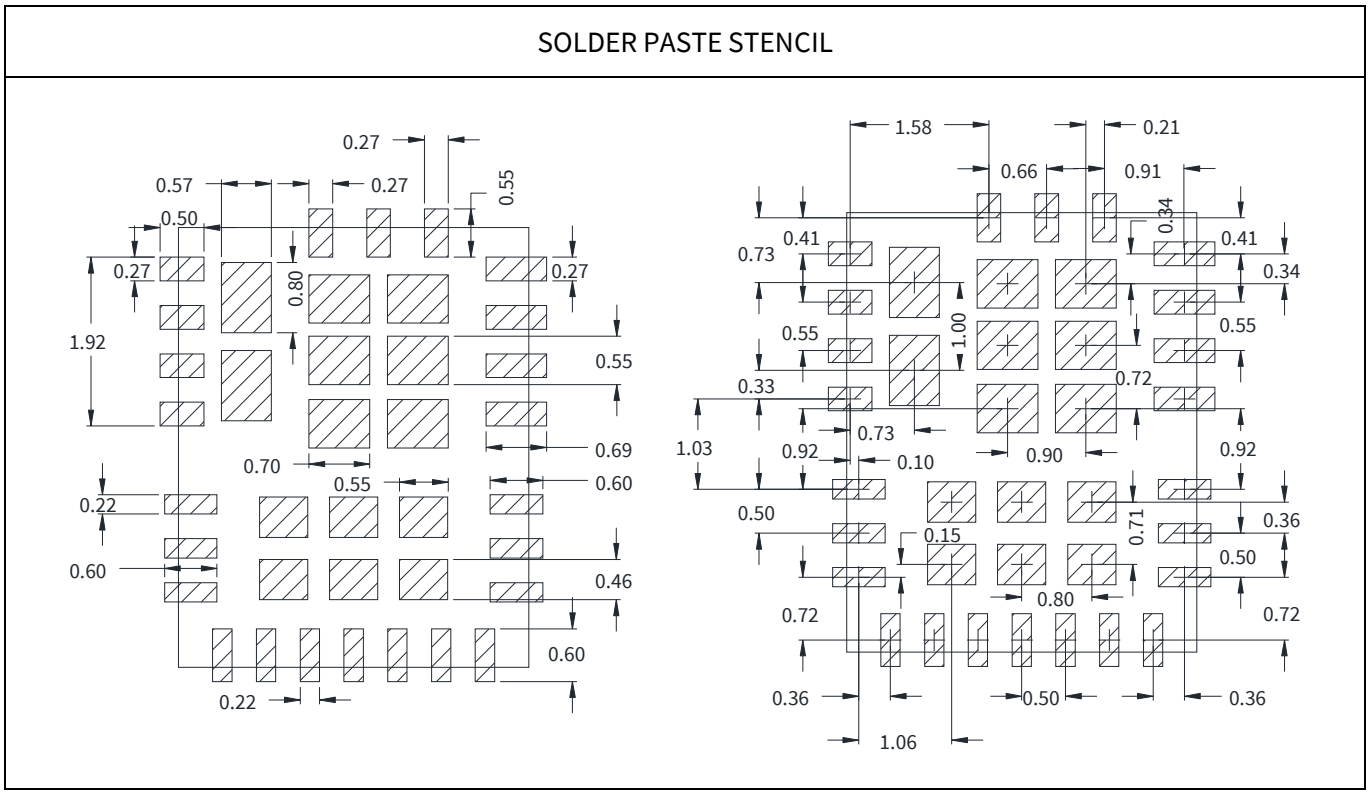


Figure 21 Stencil pad size and spacing (all dimensions in mm)

16 Package

This section includes mechanical and packaging information for the IR3899A.

16.1 Marking Information

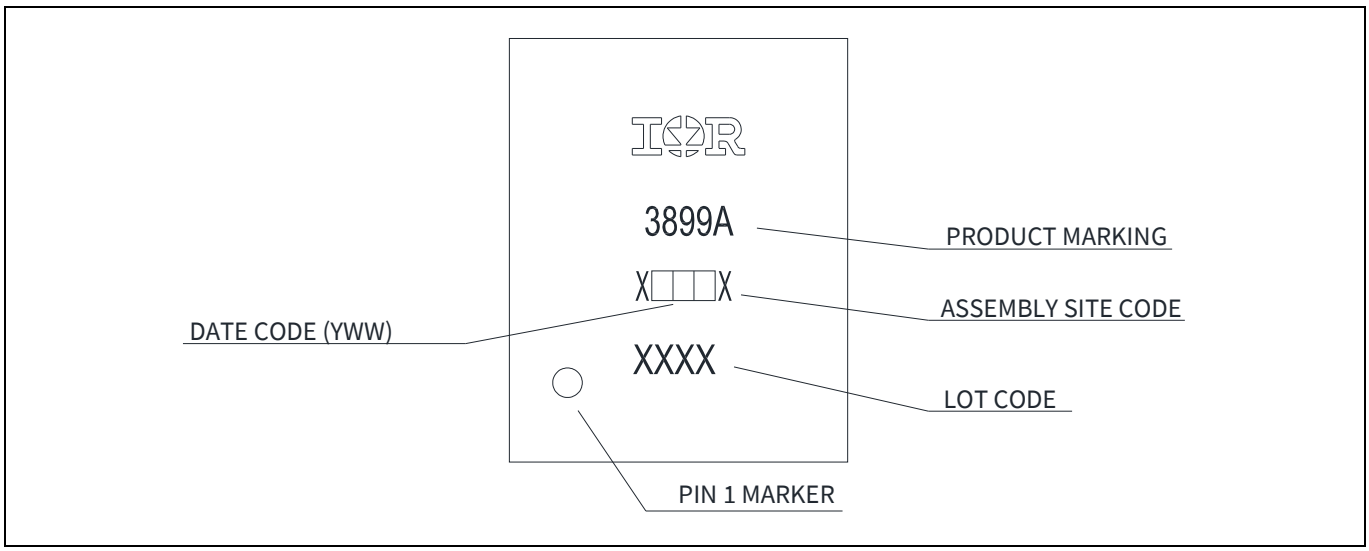
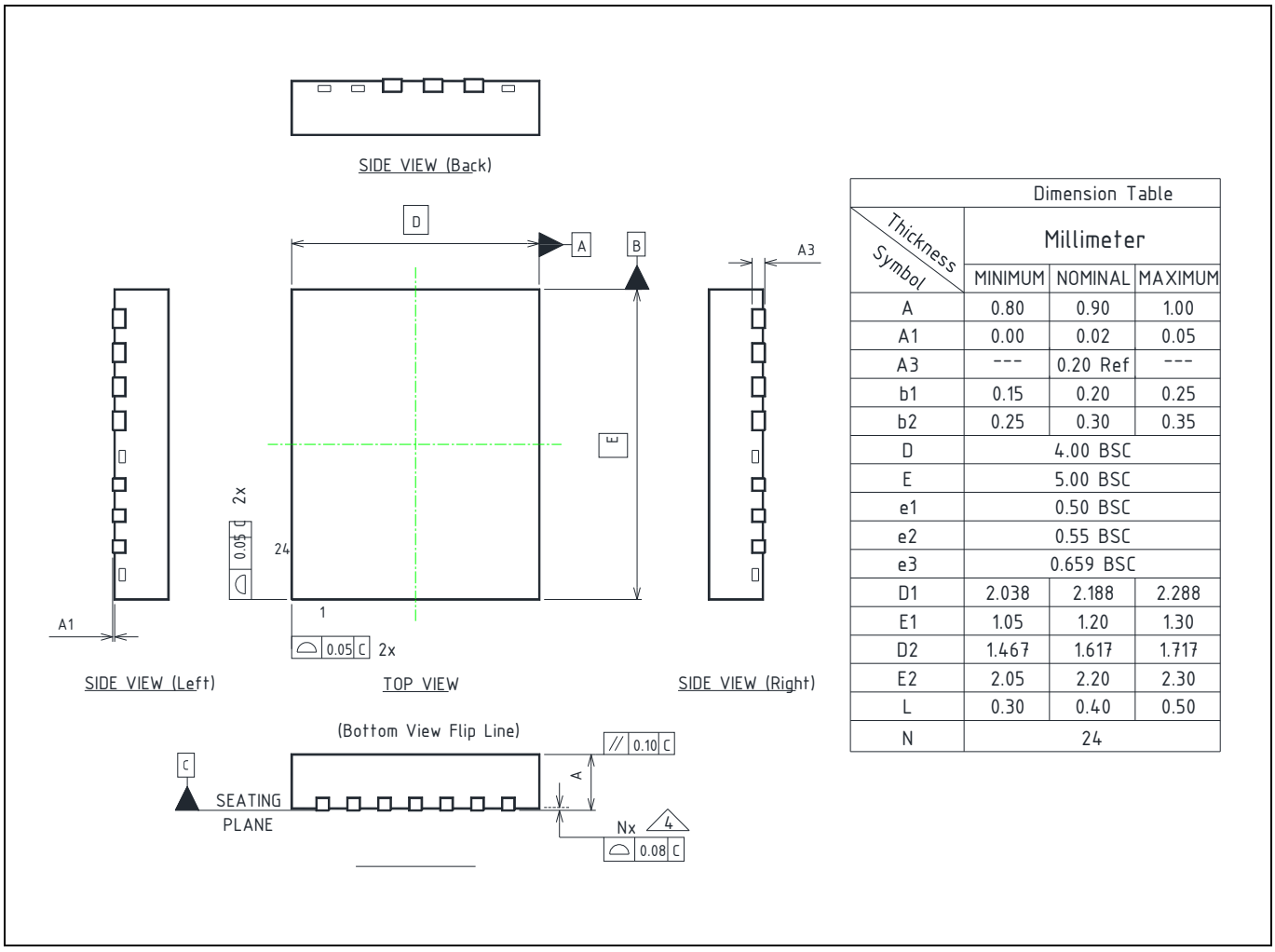


Figure 22 Package Marking

16.2 Dimensions



Dimension Table			
Thickness / Symbol	Millimeter		
	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.20 Ref	---
b1	0.15	0.20	0.25
b2	0.25	0.30	0.35
D	4.00 BSC		
E	5.00 BSC		
e1	0.50 BSC		
e2	0.55 BSC		
e3	0.659 BSC		
D1	2.038	2.188	2.288
E1	1.05	1.20	1.30
D2	1.467	1.617	1.717
E2	2.05	2.20	2.30
L	0.30	0.40	0.50
N	24		

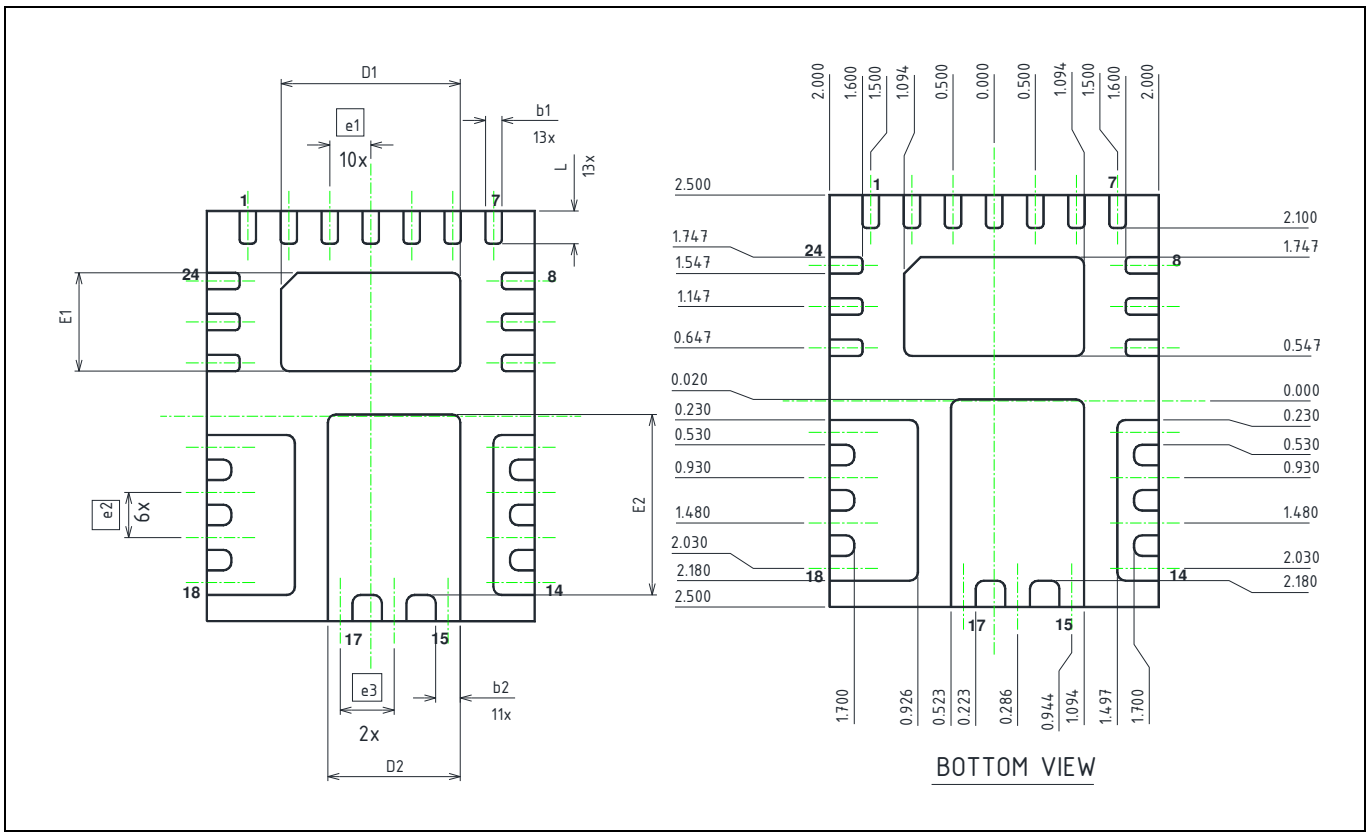


Figure 23 Package Dimensions (all dimensions in mm)

17 Environmental qualifications

Qualification Level		**Industrial**	
Moisture Sensitivity		PQFN Package	JEDEC Level 2 @ 260 °C
ESD	Human Body Model	ANSI/ESDA/JEDEC JS-001, Level 1C (1000 V to < 2000 V)	
	Charged Device Model	ANSI/ESDA/JEDEC JS-002, Level C3 (≥ 1000 V)	
RoHS Compliant		Yes	

Revision History

IR3899A

Revision: 2021-08-03, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-01-15	Release of final version
2.1	2021-05-05	(1) Max. Vout updated to 6V in recommended operating conditions; (2) Update to Note 2, 4 and added Note 5.
2.2	2021-08-03	(1) Updated Ordering Information; (2) Fixed typo in 12.9 - UVP enabled after soft start reaches 100mV.

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