

# MC74LVX138

## 3-to-8 Line Decoder

### With 5V-Tolerant Inputs

The MC74LVX138 is an advanced high speed CMOS 3-to-8 line decoder. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

When the device is enabled, three Binary Select inputs (A0 – A2) determine which one of the outputs ( $\overline{O0}$  –  $\overline{O7}$ ) will go Low. When enable input E3 is held Low or either  $\overline{E2}$  or  $\overline{E1}$  is held High, decoding function is inhibited and all outputs go high. E3,  $\overline{E2}$ , and  $\overline{E1}$  inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

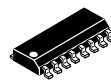
#### Features

- High Speed:  $t_{PD} = 5.5$  ns (Typ) at  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 4$   $\mu$ A (Max) at  $T_A = 25$  °C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.5$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant



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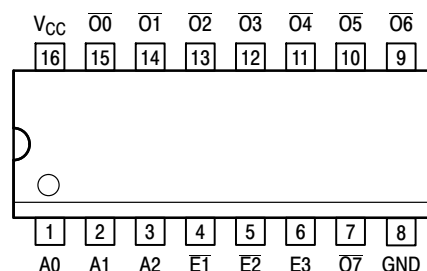


**SOIC-16  
D SUFFIX  
CASE 751B**



**TSSOP-16  
DT SUFFIX  
CASE 948F**

#### PIN ASSIGNMENT

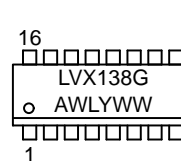


**16-Lead (Top View)**

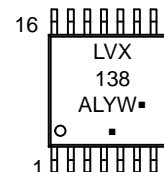
#### PIN NAMES

Pins	Function
A0–A2	Address Inputs
$\overline{E1}$ – $\overline{E2}$	Enable Inputs
E3	Enable Input
$\overline{O0}$ – $\overline{O7}$	Outputs

#### MARKING DIAGRAMS



**SOIC-16**



**TSSOP-16**

LVX138 = Specific Device Code  
 A = Assembly Location  
 WL, L = Wafer Lot  
 Y = Year  
 WW, W = Work Week  
 G or  $\blacksquare$  = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# MC74LVX138

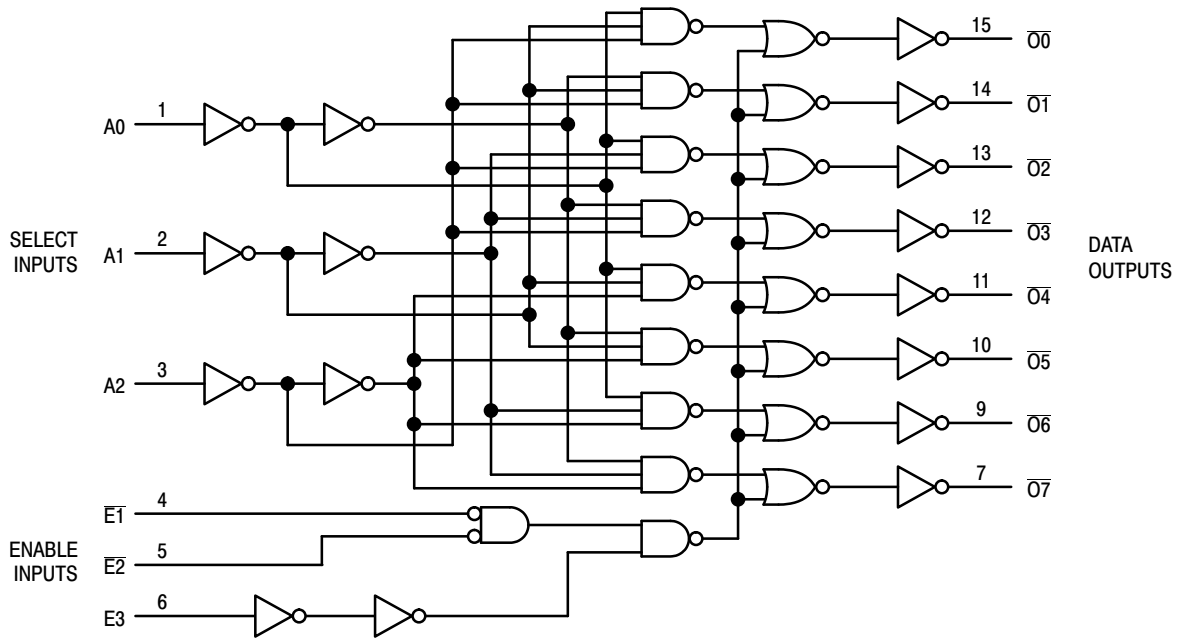


Figure 1. Logic Diagram

INPUTS						OUTPUTS							
E1	E2	E3	A0	A1	A2	O0	O1	O2	O3	O4	O5	O6	O7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H	H
L	L	H	H	H	H	H	H	H	H	H	L	H	L
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level; L = Low Voltage Level; X = High or Low Voltage Level and Transitions Are Acceptable; For I<sub>CC</sub> reasons, DO NOT FLOAT Inputs

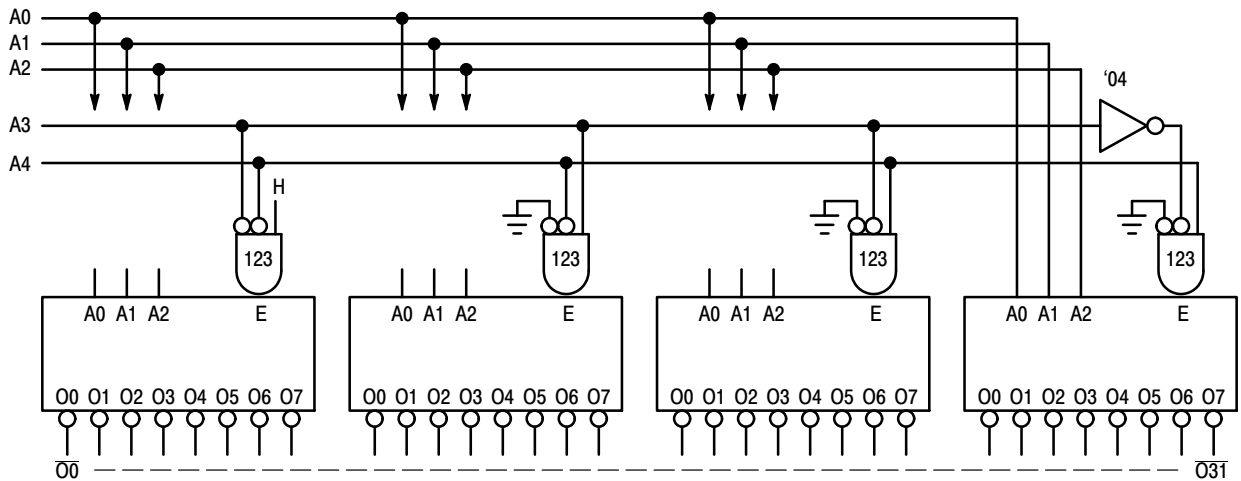


Figure 2. Expansion to 1-of-32 Decoding

# MC74LVX138

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>out</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input Diode Current	-20	mA
I <sub>OK</sub>	Output Diode Current	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation	180	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	3.6	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		2.0	1.5	-	-	1.5	-	V
			3.0	2.0	-	-	2.0	-	
			3.6	2.4	-	-	2.4	-	
V <sub>IL</sub>	Low-Level Input Voltage		2.0	-	-	0.5	-	0.5	V
			3.0	-	-	0.8	-	0.8	
			3.6	-	-	0.8	-	0.8	
V <sub>OH</sub>	High-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OH</sub> = -50μA I <sub>OH</sub> = -50μA I <sub>OH</sub> = -4mA	2.0	1.9	2.0	-	1.9	-	V
			3.0	2.9	3.0	-	2.9	-	
			3.0	2.58	-	-	2.48	-	
V <sub>OL</sub>	Low-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OL</sub> = 50μA I <sub>OL</sub> = 50μA I <sub>OL</sub> = 4mA	2.0	-	0.0	0.1	-	0.1	V
			3.0	-	0.0	0.1	-	0.1	
			3.0	-	-	0.36	-	0.44	
I <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = 5.5V or GND	3.6	-	-	±0.1	-	±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	3.6	-	-	4.0	-	40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MC74LVX138

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Input to Output	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$	–	7.1	13.8	1.0	16.5	ns
		$C_L = 50\text{pF}$	–	9.6	17.3	1.0	20.0	
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$	–	5.5	8.8	1.0	10.5	
		$C_L = 50\text{pF}$	–	8.0	12.3	1.0	14.0	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay E3 to $\bar{O}$	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$	–	8.7	16.3	1.0	19.5	ns
		$C_L = 50\text{pF}$	–	11.2	19.8	1.0	23.0	
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$	–	6.8	10.6	1.0	12.5	
		$C_L = 50\text{pF}$	–	9.3	14.1	1.0	16.0	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay E1 or E2 to $\bar{O}$	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$	–	8.8	16.0	1.0	18.5	ns
		$C_L = 50\text{pF}$	–	11.3	19.5	1.0	22.0	
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$	–	6.9	10.4	1.0	11.5	
		$C_L = 50\text{pF}$	–	9.4	13.9	1.0	15.0	
$t_{OSHL}$ , $t_{OSLH}$	Output-to-Output Skew (Note 1)	$V_{CC} = 2.7\text{V}$ $C_L = 50\text{pF}$	–	–	2.5	–	2.5	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$	–	–	2.5	–	2.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
$C_{in}$	Input Capacitance	–	4	10	–	10	pF
$C_{PD}$	Power Dissipation Capacitance (Note 2)	–	34	–	–	–	pF

2.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$ .  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ , $C_L = 50\text{pF}$ , $V_{CC} = 3.3\text{V}$ , Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	–	0.5	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	–	–0.5	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage	–	2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage	–	0.8	V

# MC74LVX138

## SWITCHING WAVEFORMS

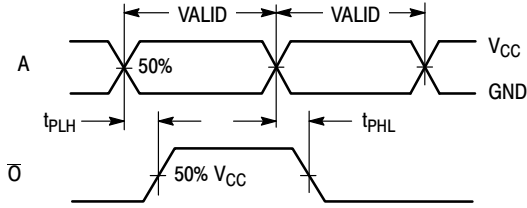


Figure 3. .

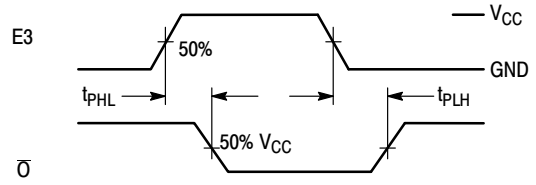


Figure 4. .

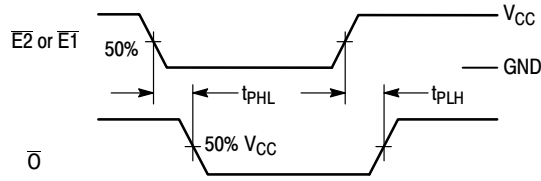
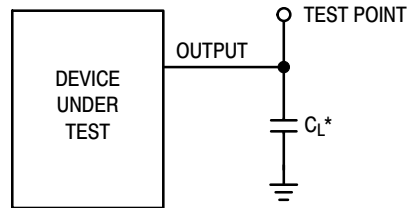


Figure 5.

## TEST CIRCUIT



\*Includes all probe and jig capacitance

Figure 6.

## ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX138DR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LVX138DTR2G	TSSOP-16 (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- |  |  |  |  |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>                           | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>   | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>                                 | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> |  |

### SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

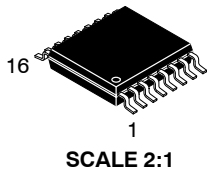
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# MECHANICAL CASE OUTLINE

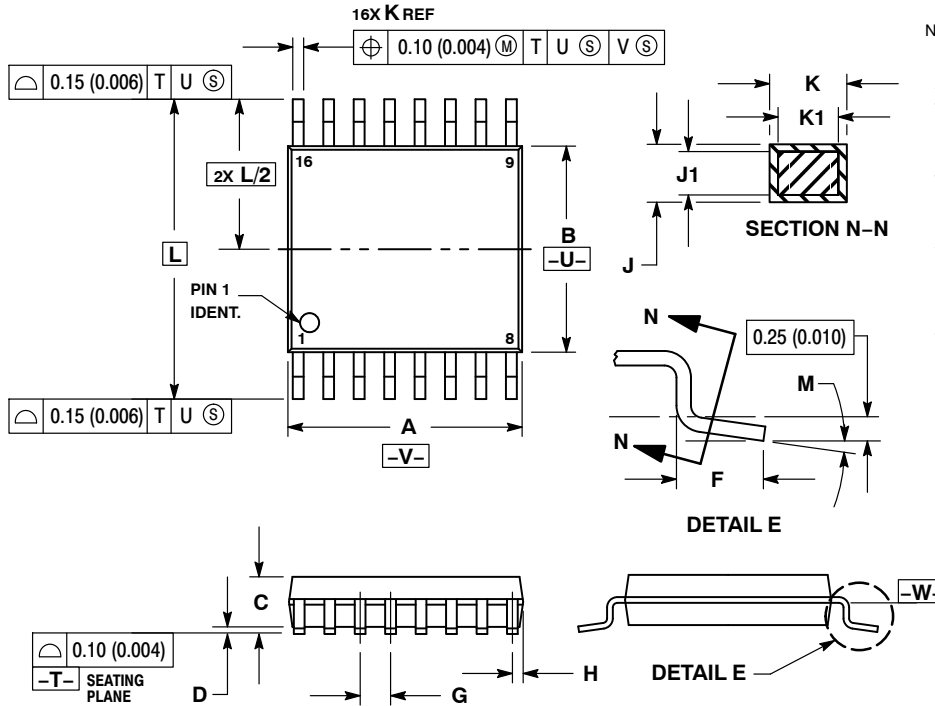
## PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16  
CASE 948F-01  
ISSUE B

DATE 19 OCT 2006

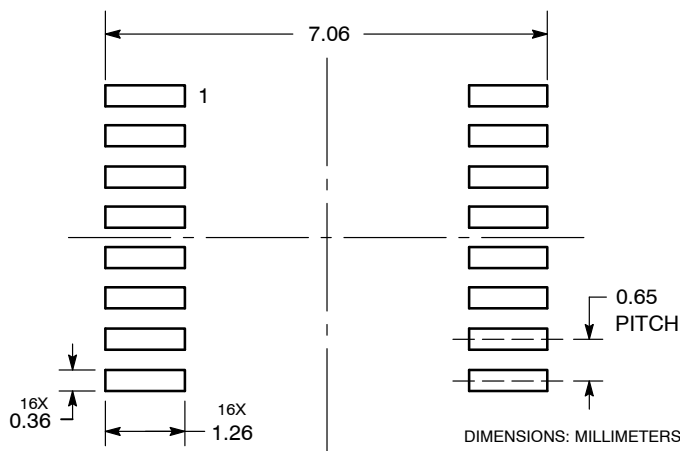


NOTES:

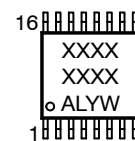
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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