SPECIFICATION

PART NO. : OEL9M0072-Y-E

This specification may be changed without any notice in order to improve performance or quality etc.
Please contact OLED R&D department TRULY Semiconductors LTD. for updated specification and product status before designing for this product or releasing the order.

PRODUCT CONTENTS

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REVISION HISTORY

Rev.	Contents	Date
0.0	Preliminary	2010-11-10
0.1	Update ELECTRO-OPTICAL CHARACTERISTICS and OUTGOING QUALITY CONTROL SPECIFICATION	2011-05-25
1.0	Update INITIALIZATION CODE and IIC INTERFACE	11-08-2011

n PHYSICAL DATA

No.	Items:	Specification:	Unit
1	Diagonal Size	1.54	Inch
2	Resolution	128(H) x 64(V)	Dots
3	Active Area	35.04(W) x 17.51(H)	mm
4	Outline Dimension (Panel)	42.04(W) x 27.22(H)	mm
5	Pixel Pitch	0.274(W) x 0.274(H)	mm
6	Pixel Size	0.249(W) x 0.249(H)	mm
7	Driver IC	SSD1305Z	-
8	Display Color	Yellow	-
9	Gray Scale	1	Bit
10	Interface	Parallel / SPI/IIC	-
11	IC package type	COG	-
12	Thickness	1.5 ± 0.1	mm
13	Weight	TBD	g
14	Duty	1/64	-

n ABSOLUTE MAXIMUM RATINGS

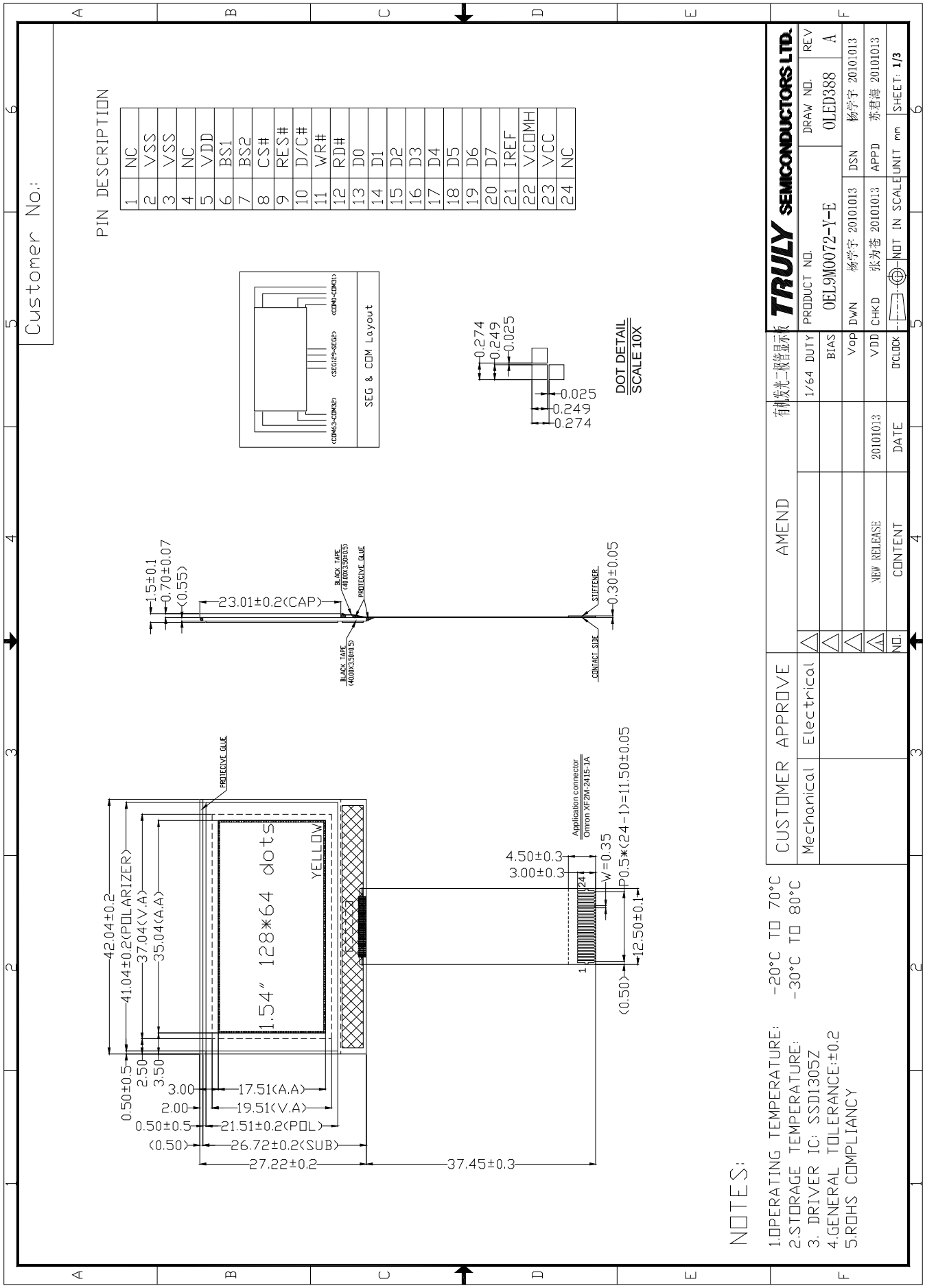
Voltage Referenced to VSS

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V_{DD}	-0.3	-	4.0	V
	Driving	V_{CC}	-0.3	-	16.0	V
Operating Temperature		Top	-20	-	70	℃
Storage Temperature		Tst	-30	-	80	℃
Humidity		-	-	-	90	%RH

NOTE:

Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

n EXTERNAL DIMENSIONS



n ELECTRICAL CHARACTERISTICS

◆ DC Characteristics

Condition (Unless otherwise specified):Voltage referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V_{DD}	2.4	3.0	3.5	V
	Operating	V_{CC}	7.0	12.0	15.0	V
Input Voltage	High Voltage	V_{IH}	0.8 x V_{DD}	-	V_{DD}	V
	Low Voltage	V_{IL}	V_{SS}	-	0.2 x V_{DD}	V
Output Voltage	High Voltage	V_{OH}	0.9 x V_{DD}	-	V_{DD}	V
	Low Voltage	V_{OL}	V_{SS}	-	0.1 x V_{DD}	V

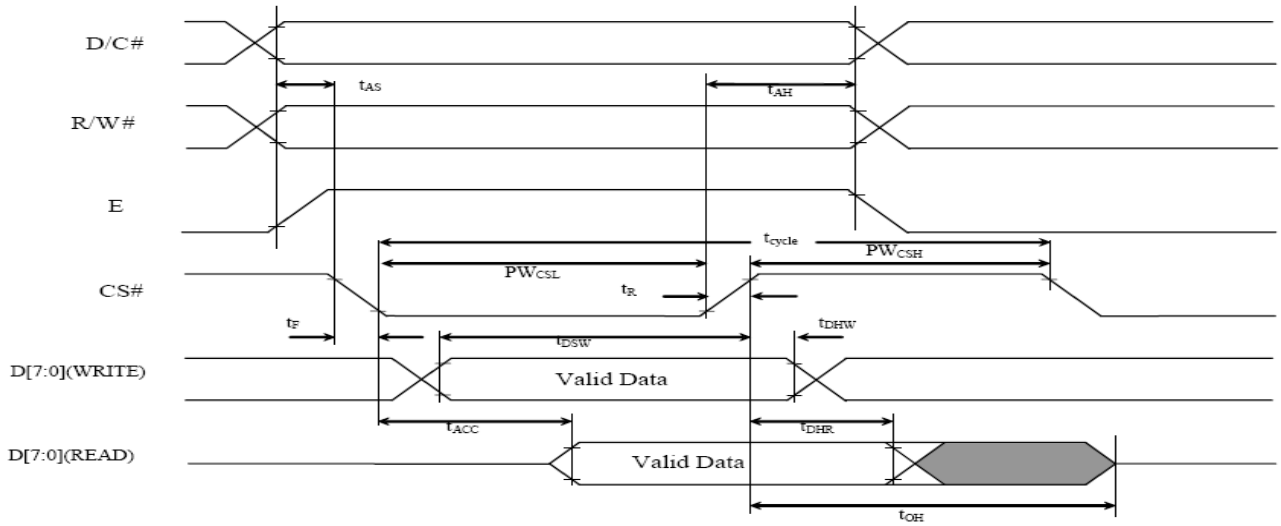
◆AC Characteristics

6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4V to 3.5V, V_{DDIO} = V_{DD}, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

6800-series MCU parallel interface characteristics



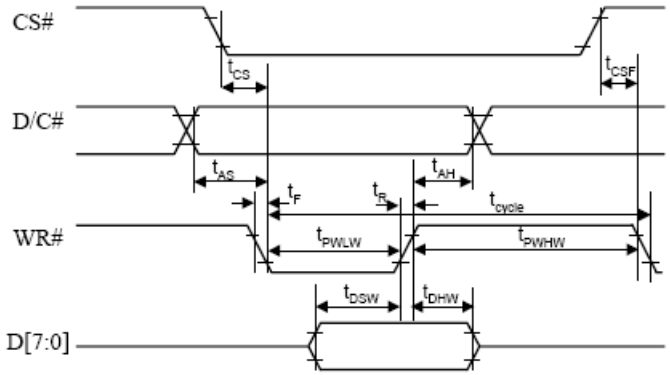
8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4V to 3.5V, V_{DDIO} = V_{DD}, T_A = 25°C)

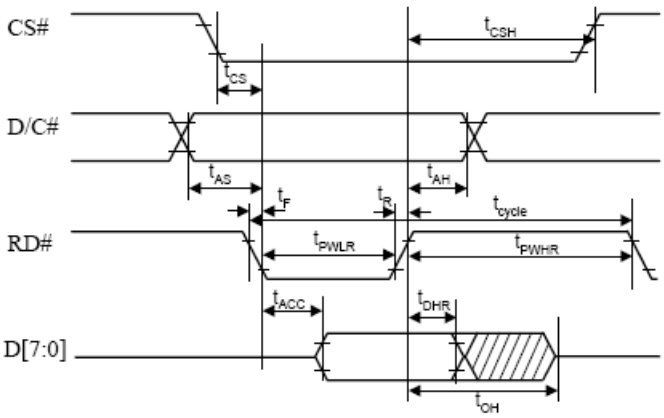
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics(Form 1)

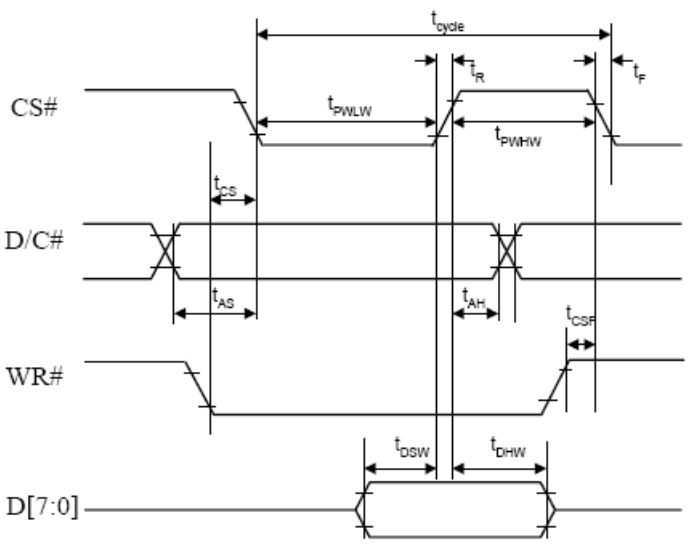
Write cycle (Form 1)

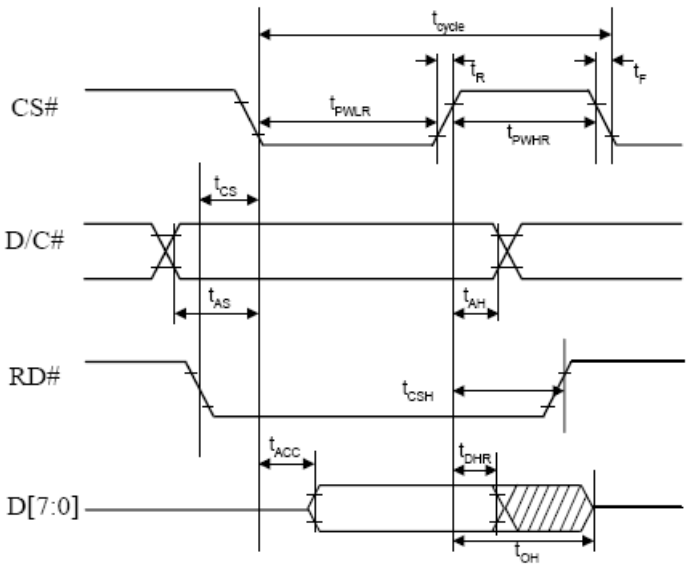


Read cycle (Form 1)



8080-series parallel interface characteristics(Form 2)



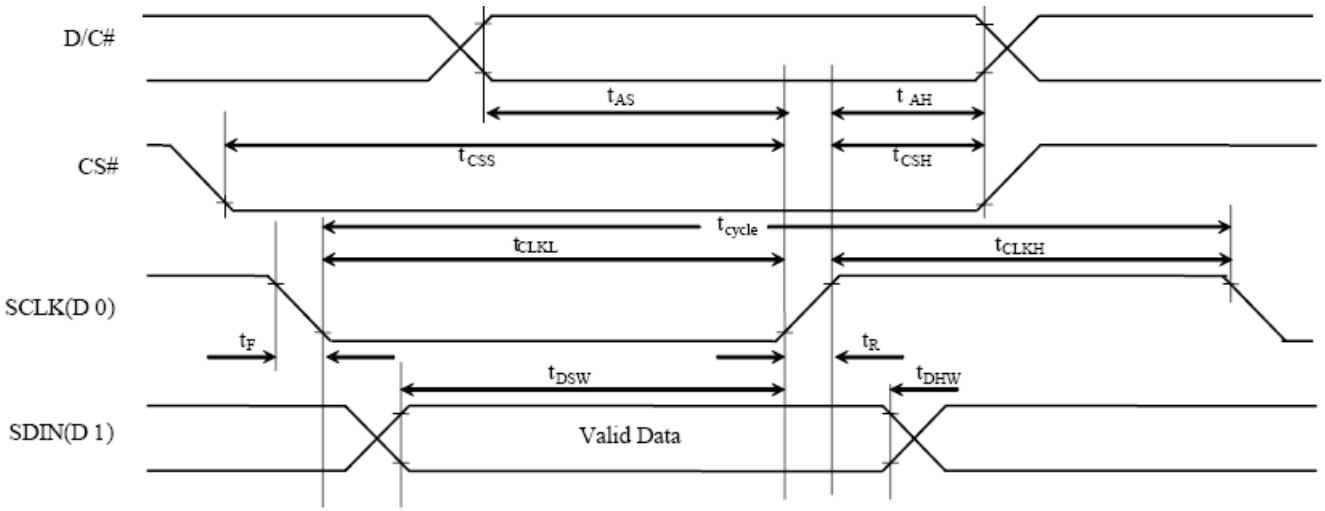


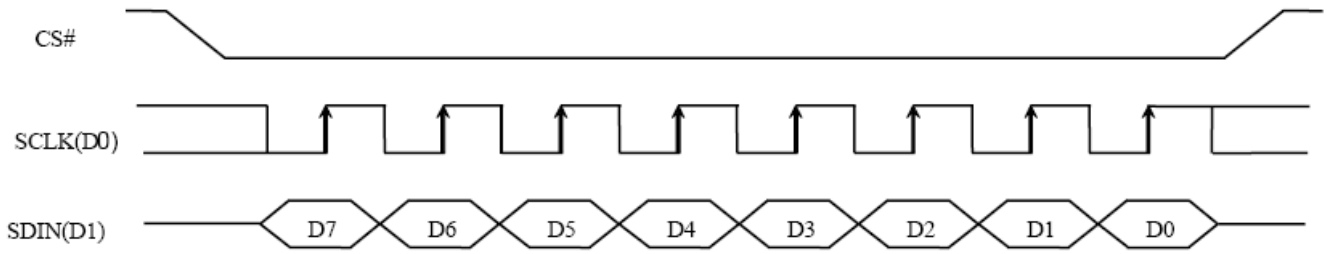
Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4V to 3.5V , V_{DDIO} = V_{DD} ,T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Serial interface characteristics



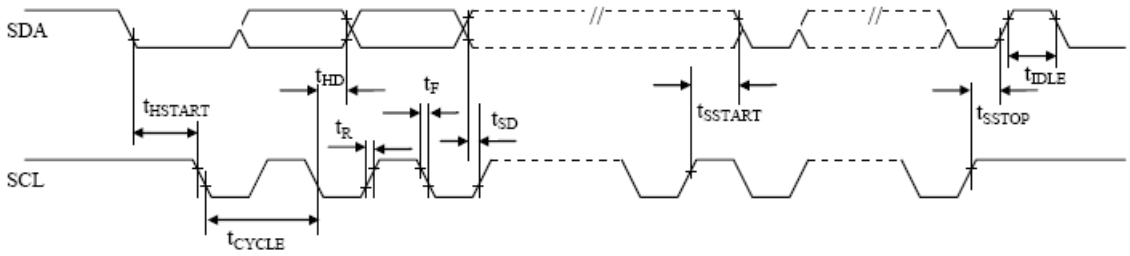


I2C Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4V to 3.5V , V_{DDIO} = V_{DD} ,T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I2C interface Timing characteristics

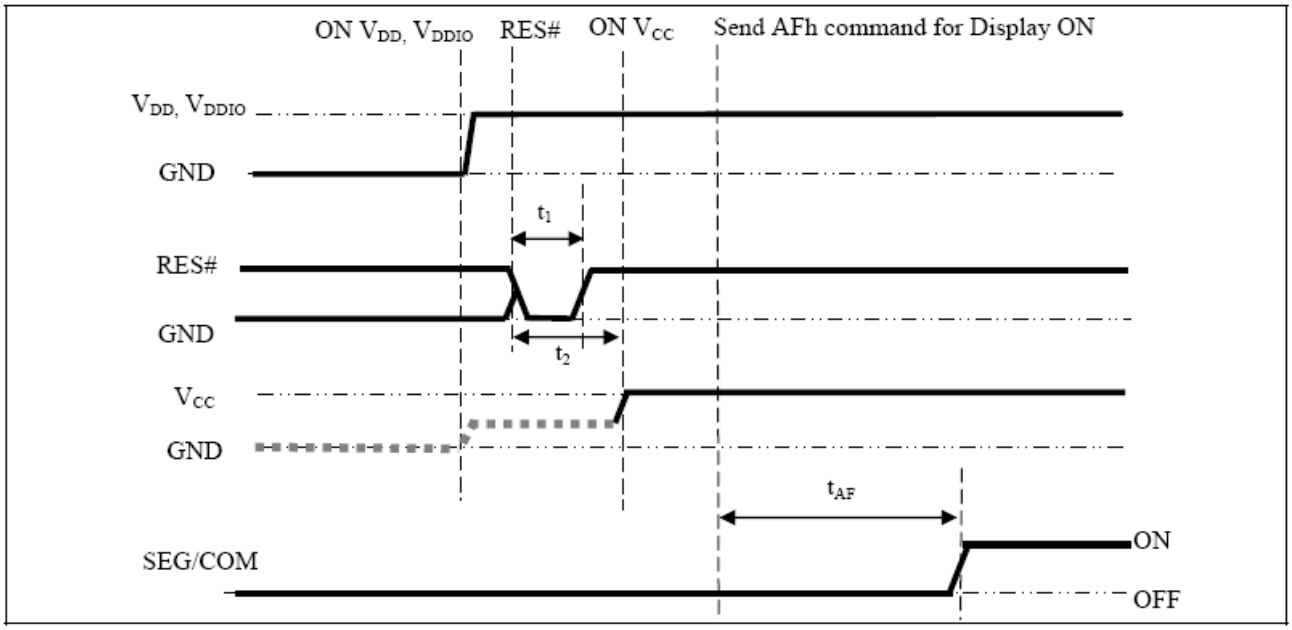


n TIMING OF POWER SUPPLY

◆*Power ON sequence*:

1. Power ON VDD,
2. After VDD become stable, set RES# pin LOW (logic low) for at least 3us(t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).

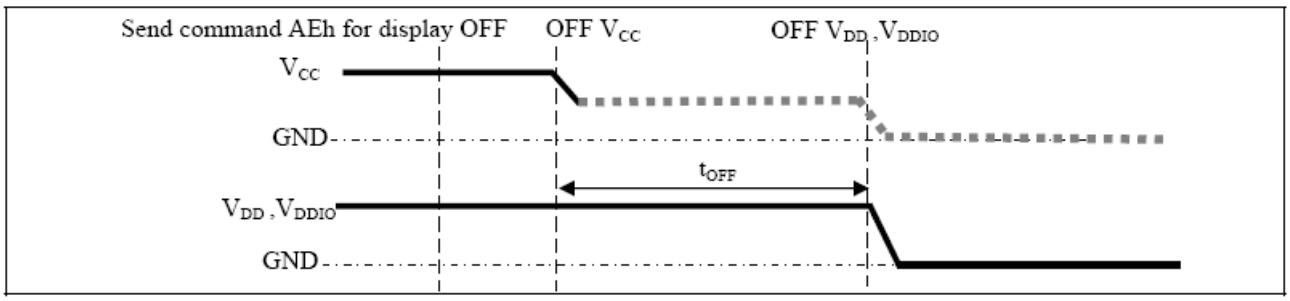
Power on sequence



◆*Power OFF sequence*:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2], [3]
3. Wait for t_{OFF}. Power OFF VDD.(where Minimum t_{OFF}=0ms [5], Typical t_{OFF}=100ms)

Power off sequence



Note:

[1] Since an ESD protection circuit is connected between VDD and V_{CC}, V_{CC} becomes lower than VDD whenever VDD is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure above.

[2] V_{CC} should be kept float (disable) when it is OFF.

[3] Power pins (VDD, V_{CC}) can never be pulled to ground under any circumstance.

[4] The register values are reset after t_1.

[5] VDD should not be Power OFF before VCC Power OFF.

n ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	80	100*	-	cd /m^2	YELLOW
Power Consumption		P	-	60	80	mW	30% pixels ON L=100 cd /m^2
Frame Frequency		Fr	-	100	-	Hz	
Color Coordinate	YELLOW	CIE x	0.42	0.46	0.50	CIE1931	Darkroom
		CIE y	0.47	0.51	0.55		
Response Time	Rise	Tr	-	-	0.02	ms	-
	Decay	Td	-	-	0.02	ms	-
Contrast Ratio*		Cr	10000:1	-	-		Darkroom
Viewing Angle Uniformity		△ θ	160	-	-	Degree	-
Operating Life Time*		Top	40,000	-	-	Hours	L=100 cd /m^2

Note:

1. **100cd/m^2** is based on V_{DD}=3.0V, V_{CC}=13.0V, contrast register value is 0x2F;
2. **Contrast ratio** is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo – detector output with OLED being “white”}}{\text{Photo – detector output with OLED being “black”}}$$

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternatively displayed)
(The initial value should be closed to the typical value after adjusting.)

n INTERFACE PIN CONNECTIONS

No	Symbol	Description
1	NC	No connection
2	VSS	Ground
3	VSS	Ground
4	NC	No connection
5	VDD	Voltage supply for core logic and interface logic.
6	BS1	MCU bus interface selection pins.Please refer to table followed for details of setting.
7	BS2	MCU bus interface selection pins.Please refer to table followed for details of setting.
8	CS#	The chip select pin. Active low.
9	RES#	This pin is reset signal input. When the pin is LOW, initialization of the chip is executed.Keep this pin HIGH (i.e. connect to VDD) during normal operation.
10	D/C#	Data/Command data control pin.Low for command while high for data.
11	WR#	This is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e.connect to VDD) and write mode when LOW.When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.When serial interface is selected, this pin must be connected to VSS.
12	RD#	When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E)signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to VDD)and the chip is selected.When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.When serial interface is selected, this pin must be connected to VSS.
13-20	D0-D7	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be left opened.When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
21	IREF	This is segment output current reference pin.A resistor should be connected between this pin and VSS to maintain the IREF current at 10uA.
22	VCOMH	The pin for COM signal deselected voltage level.A capacitor should be connected between this pin and VSS.
23	VCC	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
24	NC	No connection

MCU Bus Interface Pin Selection

Pin Name	I2C Interface	6800- parallel interface(8 bit)	8080- parallel Interface (8 bit)	Serial interface
BS1	1	0	1	0
BS2	0	1	1	0

n COMMAND TABLE

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[7:0] : Column start address, range : 0-131d, (RESET=0d) B[7:0]: Column end address, range : 0-131d, (RESET =131d)
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d)
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control For BANK0	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 80h)
0 0	82 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Brightness For Area Color Banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (RESET = 80h)
0 0 0 0 0	91 X[5:0] A[5:0] B[5:0] C[5:0]	1 * * * *	0 * * * *	0 X_5 A_5 B_5 C_5	1 X_4 A_4 B_4 C_4	0 X_3 A_3 B_3 C_3	0 X_2 A_2 B_2 C_2	0 X_1 A_1 B_1 C_1	1 X_0 A_0 B_0 C_0	Set Look Up Table (LUT)	Set current drive pulse width of BANK0, Color A, B and C. BANK0: X[5:0] = 31… 63; for pulse width set to 32 ~ 64 clocks (RESET = 110001b) Color A: A[5:0] same as above (RESET = 111111b) Color B: B[5:0] same as above (RESET = 111111b) Color C: C[5:0] same as above (RESET = 111111b) Note (1) Color D pulse width is fixed at 64 clocks pulse.

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0 0 0	92 A[7:0] B[7:0] C[7:0] D[7:0]	1 A_7 B_7 C_7 D_7	0 A_6 B_6 C_6 D_6	0 A_5 B_5 C_5 D_5	1 A_4 B_4 C_4 D_4	0 A_3 B_3 C_3 D_3	0 A_2 B_2 C_2 D_2	1 A_1 B_1 C_1 D_1	0 A_0 B_0 C_0 D_0	Set Bank Color of BANK1 to BANK16 (PAGE0)	Set the bank color of BANK1~BANK16 to any one of the 4 colors : A, B, C and D . A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK1 A[3:2] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK2 : : D[5:4]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK15 D[7:6]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK16
0 0 0 0 0	93 A[7:0] B[7:0] C[7:0] D[7:0]	1 A_7 B_7 C_7 D_7	0 A_6 B_6 C_6 D_6	0 A_5 B_5 C_5 D_5	1 A_4 B_4 C_4 D_4	0 A_3 B_3 C_3 D_3	0 A_2 B_2 C_2 D_2	1 A_1 B_1 C_1 D_1	1 A_0 B_0 C_0 D_0	Set Bank Color of BANK17~BANK32 (PAGE1)	Set the bank color of BANK17~BANK32 to any one of the 4 colors: A, B, C and D. A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK17 A[3:2] : 00b, 01b, 10b, or 1b1 for Color = A, B, C or D of BANK18 : : D[5:4]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK31 D[7:6]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK32
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	X[0]=0b: column address 0 is mapped to SEG0 (RESET) X[0]=1b: column address 131 is mapped to SEG0
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	X_0=0b: Resume to RAM content display (RESET) Output follows RAM content X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel X[0]=1b: inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	AA	1	0	1	0	1	0	1	0	Reserved	Reserved
0 0 0 0	AB A[3:0] B[7:0] C[7:0]	1 * B_7 C_7	0 * B_6 C_6	1 * B_5 C_5	0 * B_4 C_4	1 A_3 B_3 C_3	0 A_2 B_2 C_2	1 A_1 B_1 C_1	1 A_0 B_0 C_0	Dim mode setting	A[3:0] : Reserved (set as 0000b) B [7:0] : Set contrast for BANK0, valid range 0-255d, please refer to command 81h C [7:0] : Set brightness for color bank, valid range 0-255d, please refer to command 82h

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	AD A[7:0]	1 1	0 0	1 0	0 0	1 1	1 1	0 1	1 A_0	Master Configuration	A[0]=0b, Select external V_{CC} supply (RESET) A[0]=1b, Reserved
0	AC AE AF	1	0	1	0	1	1	A_1	A_0	Set Display ON/OFF	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) (RESET) AFh = Display ON in normal mode
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0].
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] X[3]=1b: remapped mode. Scan from COM[N~1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0~63. The value is reset to 00h after RESET.
0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b Range:0000b~1111b Frequency increases as setting value increases. Refer to section 10.1.23 for details.
0 0	D8	1 0	1 0	0 X_5	1 X_4	1 0	0 X_2	0 0	0 X_0	Set Area Color Mode ON/OFF & Low Power Display Mode	X[5:4]= 00b (RESET) : monochrome mode X[5:4]= 11b Area Color enable X[2]=0b and X[0]=0b: Normal power mode(RESET) X[2]=1b and X[0]=1b: Set low power display mode
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks (RESET=2h); 0 is invalid entry A[7:4] : Phase 2 period of up to 15 DCLK clocks (RESET=2h); 0 is invalid entry
0 0	DA	1 0	1 0	0 X_5	1 X_4	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	X[4]=0b, Sequential COM pin configuration X[4]=1b(RESET), Alternative COM pin configuration X[5]=0b(RESET), Disable COM Left/Right remap X[5]=1b, Enable COM Left/Right remap Please refer to Table 10-3 for details.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	DB A[5:2]	1 0	1 0	0 A_5	1 A_4	1 A_3	0 A_2	1 0	1 0	Set V_{COMH} Deselect Level	A[5:2] / Hex code / V_{COMH} deselect level 0000b / 00h / ~ 0.43 x V_{CC} 1101b / 34h / ~ 0.77 x V_{CC} (RESET) 1111b / 3Ch / ~ 0.83 x V_{CC}
0	E0	1	1	1	0	0	0	0	0	Enter Read Modify Write	Enter the Read Modify Write mode. Details please refer to section 10.1.28.
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation
0	EE	1	1	1	0	1	1	1	0	Exit Read Modify Write	Exit the Read Modify Write mode (Please refer to command E0h)

Graphic Acceleration Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0	0	1	1	X_0	Horizontal Scroll Setup	X[0]=0, Right Horizontal Scroll X[0]=1, Left Horizontal Scroll A[2:0] : Set number of column scroll offset 000b No horizontal scroll 001b Horizontal scroll by 1 column 010b Horizontal scroll by 2 columns 011b Horizontal scroll by 3 columns 100b Horizontal scroll by 4 columns Other values are invalid. B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 6 frames | 100b – 3 frames 001b – 32 frames | 101b – 4 frames 010b – 64 frames | 110b – 2 frame 011b – 128 frames | 111b – Invalid D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 The value of D[2:0] must be larger or equal to B[2:0]
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	29/2A	0	0	1	0	1	0	X_1	X_0	Continuous Vertical and Horizontal Scroll Setup	X_1X_0=01b : Vertical and Right Horizontal Scroll X_1X_0=10b : Vertical and Left Horizontal Scroll A[2:0] : Set number of column scroll offset 000b No horizontal scroll 001b Horizontal scroll by 1 column 010b Horizontal scroll by 2 columns 011b Horizontal scroll by 3 columns 100b Horizontal scroll by 4 columns Other values are invalid. B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 6 frames | 100b – 3 frames 001b – 32 frames | 101b – 4 frames 010b – 64 frames | 110b – 2 frame 011b – 128 frames | 111b – Invalid D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 The value of D[2:0] must be larger or equal to B[2:0] E[5:0] : Vertical scrolling offset e.g. E[5:0]= 01h refer to offset =1 row E[5:0] =3Fh refer to offset =63 rows
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		

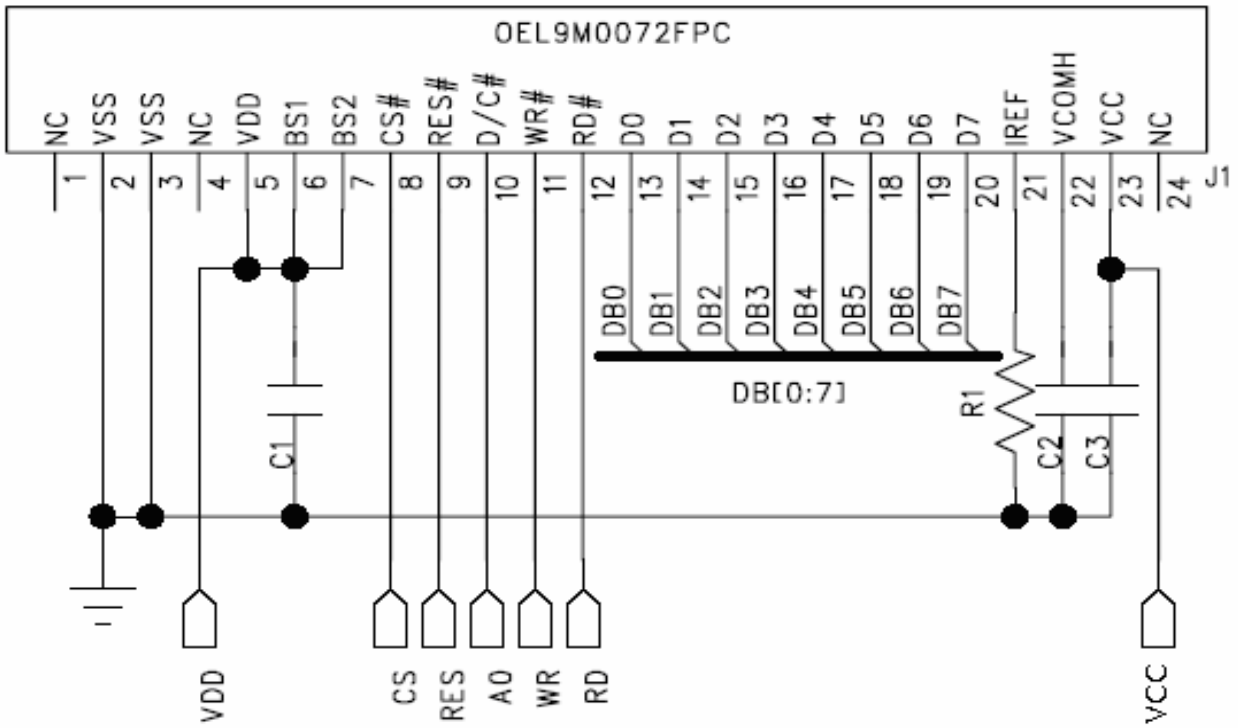
Graphic Acceleration Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh. For example, if "26h; 2Ah; 2Fh." commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.
0 0 0	A3 A[5:0] B[6:0]	1 * *	0 * B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64] **Note** (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line (X5X4X3X2X1X0 of 40h~7Fh) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0]= 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls Please refer to Figure 10-14 for details.

n INITIALIZATION CODE

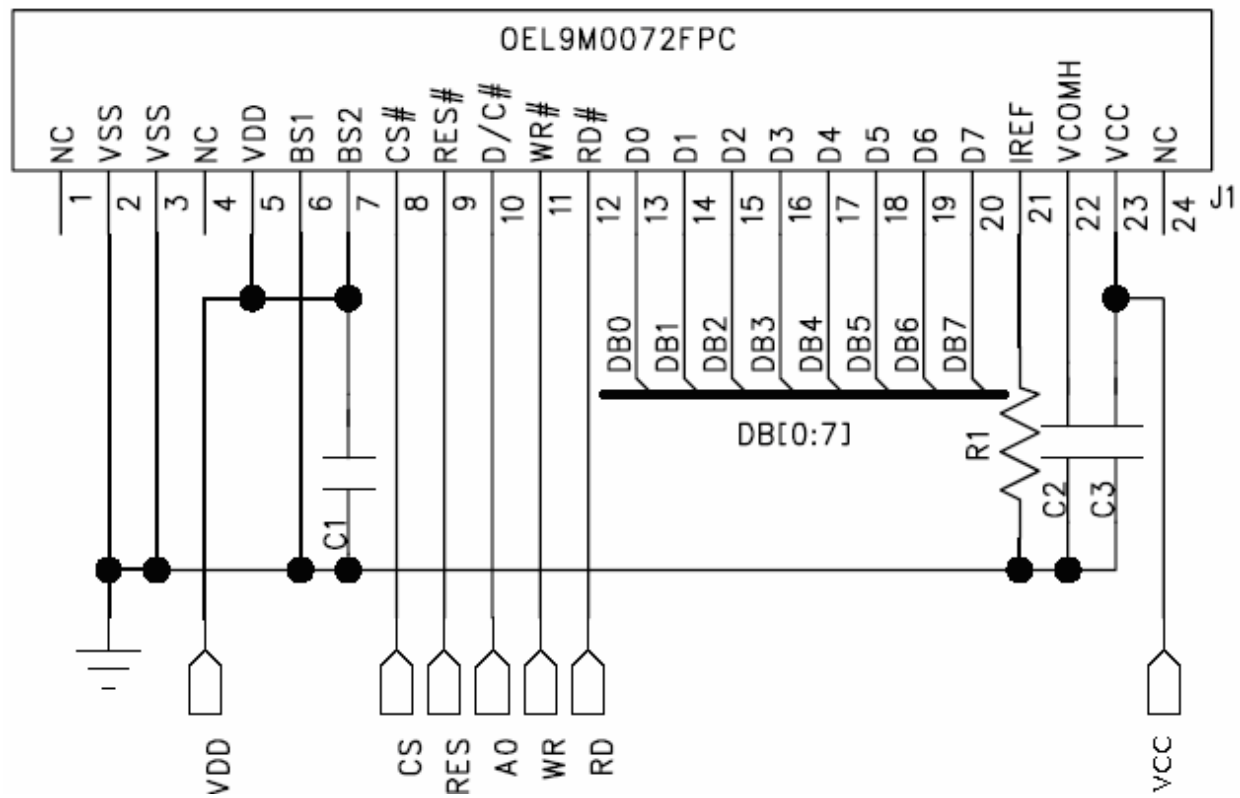
```
void InitOLED_MASTER_SSD1305(void)
{
 MainOLED_WCom(0xAE);          //DSPLAY OFF
 MainOLED_WCom(0x02);          // SET LOW START ADDRESS
 MainOLED_WCom(0x10);          // SET HIGH STAET ADDRESS
 MainOLED_WCom(0x20);          //SET MEMORRY MODE
 MainOLED_WCom(0x02);          //PAGE MODE
 MainOLED_WCom(0x21);          //SET COLUME ADDRESS
 MainOLED_WCom(0x02);          //START ADDRESS
 MainOLED_WCom(0x81);          //END ADDRESS
 MainOLED_WCom(0x22);          //SET PAGE ADDRESS
 MainOLED_WCom(0x00);
 MainOLED_WCom(0x07);
 MainOLED_WCom(0x40);          //DISPALY START LINES
 MainOLED_WCom(0x81);          //SET CONTRAST FOR BANK0
 MainOLED_WCom(CONTRAST);
 MainOLED_WCom(0x82);          //BRIGHTESS FOR COLOR BANK(NO AFFECT THE CONTRAST)
 MainOLED_WCom(0x80);
 MainOLED_WCom(0x91);          //SET LUT FOR AREA COLOR  (SET CURRENT DIRIVER PULSE WIDTH)
 MainOLED_WCom(0x3F);          //BANK 0
 MainOLED_WCom(0x00);          //COLOR A
 MainOLED_WCom(0x00);          //COLOR B
 MainOLED_WCom(0x00);          //COLOR C//***
 MainOLED_WCom(0x92);          //SET BANK 1-16 MATCH TO WHICH COLOR A,B,C,D
 MainOLED_WCom(0x00);          //00=A,01=B,10=C,11=D
 MainOLED_WCom(0x00);
 MainOLED_WCom(0x00);
 MainOLED_WCom(0x00);
 MainOLED_WCom(0x93);          //SET BANK 17-32 MATCH TO WHICH COLOR A,B,C,D
 MainOLED_WCom(0x00);          //00=A,01=B,10=C,11=D
 MainOLED_WCom(0x00);
 MainOLED_WCom(0x00);
 MainOLED_WCom(0x00);
 MainOLED_WCom(0xA0);          //SET SEG RE-MAP
 MainOLED_WCom(0xA4);          //ENTRIE DISPLAY ON
 MainOLED_WCom(0xA6);          //SET NORMAL/INVERSE DISPLAY
 MainOLED_WCom(0xA8);          //SET MULTIPLEX RADIO
 MainOLED_WCom(0x3F);
 MainOLED_WCom(0xAD);          //MASTER CONFIGURATION
 MainOLED_WCom(0x8E);          //EXTERNAL VCC
 MainOLED_WCom(0xC0);          //SET COM SCAN DIRECTION
 MainOLED_WCom(0xD3);          //SET DISPALY OFFSET
 MainOLED_WCom(0x00);          //
 MainOLED_WCom(0xD5);          //SET FREQUENCY
 MainOLED_WCom(0xf0);          //
 MainOLED_WCom(0xD8);          //SET AREA COLOR/MONO MODE  & Low power display mode
 MainOLED_WCom(0x05);          //
 MainOLED_WCom(0xD9);          //SET PRE-CHARGE Period
 MainOLED_WCom(0xf1);          //
 MainOLED_WCom(0xDA);          //SET COM PINS CONFIGURATION
 MainOLED_WCom(0x12);          //
 MainOLED_WCom(0xDB);          //SET Vcomh select level
 MainOLED_WCom(0x34);          //
 MainOLED_WCom(0xAF);          //DISPLAY ON
}
```

n SCHEMATIC EXAMPLE

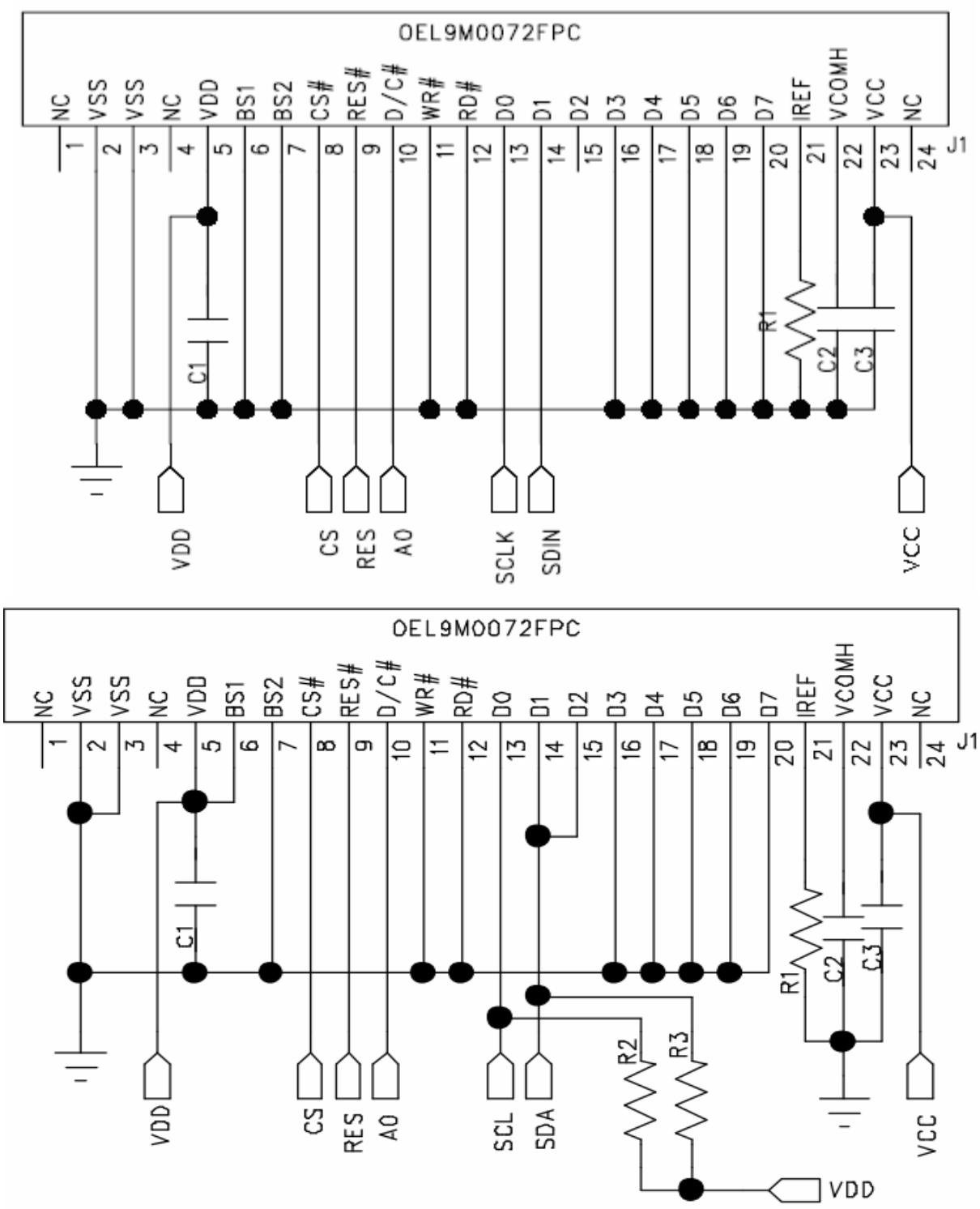
8080- parallel Interface



6800- parallel Interface



4-WIRE SPI Interface



C1: 4.7 **uF** (1)
C2: 4.7 **uF** (1)
C3: 4.7 **uF** (1)
R1: 910kΩ, R1= (Voltage at IREF pin-VSS)/IREF
R2,R3: 2K ohm (1)
Voltage at IREF pin = VCC-3V

(1) The capacitor and resistor value is recommended value. Select appropriate value against module application.

n RELIABILITY TESTS

Item		Condition	Criterion
High Temperature Storage (HTS)		80±2℃, 200 hours	1. After testing, the function test is ok. 2. After testing, no addition to the defect. 3. After testing, the change of luminance should be within +/- 50% of initial value. 4. After testing, the change for the mono and area color must be within (+/-0.02, +/-0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within +/- 50% of initial value.
High Temperature Operating (HTO)		70±2℃, 96 hours	
Low Temperature Storage (LTS)		-30±2℃, 200 hours	
Low Temperature Operating (LTO)		-20±2℃, 96 hours	
High Temperature / High Humidity Storage (HTHHS)		50±3℃, 90%±3%RH, 120 hours	
Thermal Shock (Non-operation) (TS)		-20±2℃ ~ 25℃ ~ 70±2℃ (30min) (5min) (30min) 10cycles	
Vibration (Packing)	10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z	1. One box for each test. 2. No addition to the cosmetic and the electrical defects.	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		
ESD (finished product housing)	±4kV (R: 330Ω C: 150pF , 10times, air discharge)	1. After testing, cosmetic and electrical defects should not happen. 2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.	

Note： 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).
3) The test should be done after 2 hours of recovery time in normal environment.

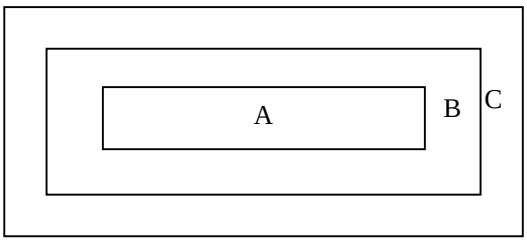
n OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

According to GB/T2828.1-2003/ISO 2859-1： 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

1 Major defect : The defect that greatly affect the usability of product.
2 Minor defect : The other defects, such as cosmetic defects, etc.
3 Definition of inspection zone:



Zone A: Active Area

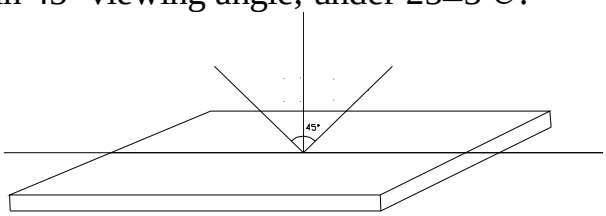
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

◆Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



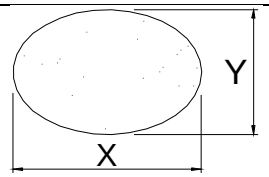
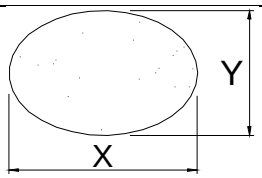
2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

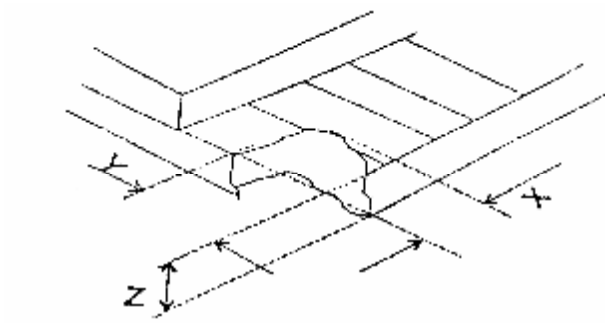
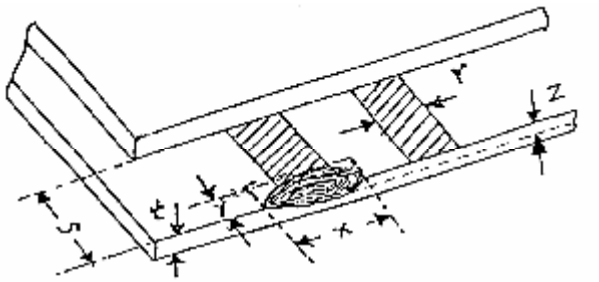
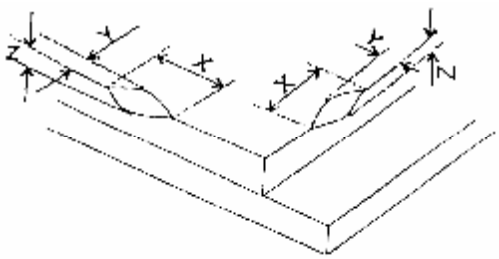
◆Inspection Criteria

1 Major defect : AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect : AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="5">Spot Defect (dimming and lighting spot)</td><td colspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td colspan="2"></td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.07</td><td colspan="2">Ignored</td></tr>
<tr><td>0.07＜Φ≦0.10</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.10＜Φ≦0. 15</td><td>1</td></tr>
<tr><td>0.15＜Φ</td><td>0</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.03＜W≦0.05</td><td>1</td></tr>
<tr><td>/</td><td>0.05＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs. The distance between two lines defects must exceed 1 mm</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="7">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignore</td></tr>
<tr><td>3.0＜L≦5.0</td><td>0.02＜W≦0.04</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦3.0</td><td>0.04＜W≦0.06</td><td>1</td></tr>
<tr><td>/</td><td>0.06＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.30</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.30＜Φ≦0.50</td><td>1</td></tr>
<tr><td>0.50＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
 
(mm)
<table><tr><td>x</td><td>≤ 1.5</td></tr><tr><td>y</td><td>≤ 1.5</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
 
(mm)
<table><tr><td>x</td><td>≤ a / 4</td></tr><tr><td>y</td><td>≤ s / 3 &≤0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
 
(mm)
<table><tr><td>x</td><td>≤ a / 8</td></tr><tr><td>y</td><td>≤ 0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

n CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{CC}$, and power off sequence: $V_{CC} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module’ s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

13.When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) TRULY will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with TRULY OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of TRULY is limited to repair and/or replacement on the terms above. TRULY will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

◆PRIOR CONSULT MATTER

1. For TRULY standard products , we keep the right to change material ,process … for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.