RAA212421

3V to 40V Input, 1.1A Synchronous Buck Regulator with Integrated 500mA LDO

FN9309
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The RAA212421 is a dual-output regulator combining a 3V to 40V input, 1.1A synchronous buck converter with a 500mA LDO featuring fast transient response. The combination of two high-performance power supplies in one compact 3x6mm package provide an easy-to-use, high-efficiency compact solution.

The wide VIN buck regulator of the RAA212421 integrates both high-side and low-side nMOSFETs and features a PFM mode for improved efficiency at light load. This feature can be disabled if forced PWM mode is desired. It can use internal or external compensation, which minimizes the required external components, reduces BOM count and complexity of design. The part switches at a default frequency of 500kHz; however, it can also be programmed using an external resistor from 300kHz to 2MHz. Other features include programmable soft-start, hiccup mode overcurrent protection, thermal shutdown, and power-good.

The LDO also features state-of-the-art internal compensation that allows it to achieve very fast load transient response. The device provides an output accuracy of ±1.8% V_{OUT} accuracy over all load, line, and temperature variations (T_J = -40°C to +125°C). Other features include soft-start and enable that allow the LDO to be placed into low quiescent current shutdown mode.

The part is available in a small Pb-free 3mm x 6mm DFN plastic package with a full-range industrial temperature of -40°C to +125°C.

Related Literature

For a full list of related documents, visit our website:

- RAA212421 device page

Features

- Wide input voltage range of 3V to 40V
- Synchronous operation for high efficiency
- Integrated high-side and low-side NMOS devices
- Selectable PFM or PWM mode at light loads
- Internal fixed frequency (500kHz) or adjustable switching frequency (300kHz to 2MHz)
- Continuous output current up to 1.1A
- Internal or external soft-start
- Power-good and enable functions
- 500mA low dropout linear regulator
- 1.8V to 6V input
- ±1.8% V_{OUT} accuracy ensured over line, load, and T_J = -40°C to +125°C
- Very low 45mV dropout voltage at V_{OUT} = 2.5V
- Excellent PSRR over wide frequency range
- Programmable output soft-start time
- Very fast transient response
- Current limit protection

Applications

- Industrial control, medical devices, portable instrumentation, distributed power supplies, cloud infrastructure

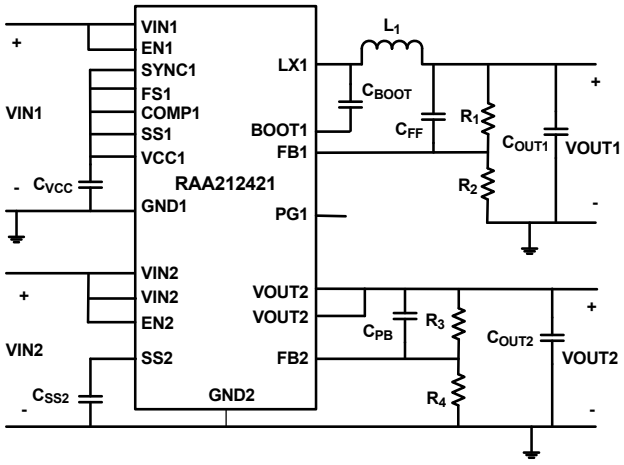

Figure 1. Typical Application

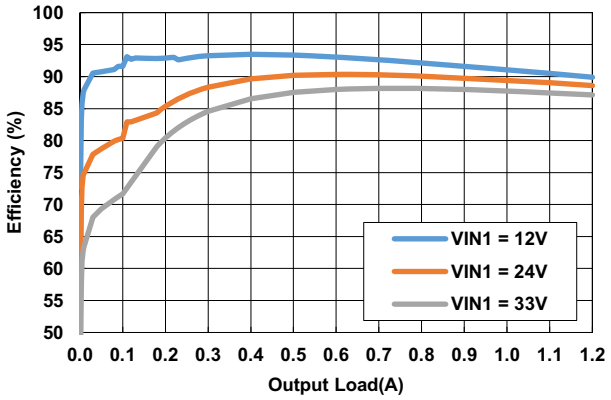

Figure 2. Efficiency vs Load, PFM, V_{OUT} = 5V, L_1 = 22µH

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1. Overview

1.1 Typical Application Circuits

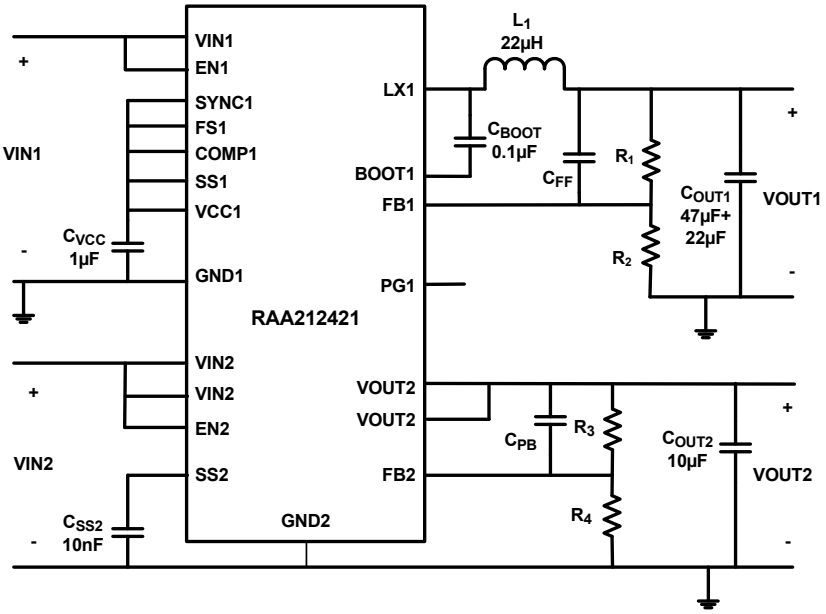


Figure 3. Internal Default Parameter Selection

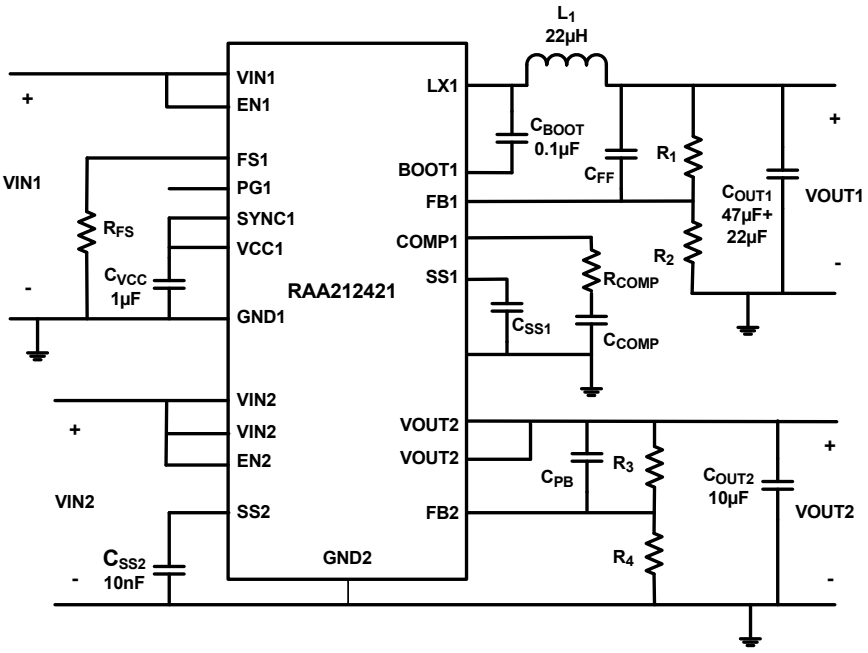


Figure 4. User Programmable Parameter Selection

Table 1. External Component Selection

V_{OUT1} (V)	L_1 (µH)	C_{OUT1} (µF)	R_1 (kΩ)	R_2 (kΩ)	C_{FF} (pF)	R_{FS} (kΩ)	R_{COMP} (kΩ)	C_{COMP} (pF)
12	33	2 x 22	90.9	4.75	4.7	115	200	470
5	22	47 + 22	90.9	12.4	22	DNP (Note 1)	130	470
3.3	22	47 + 22	90.9	20	22	DNP (Note 1)	120	470
2.5	15	47 + 22	90.9	28.7	22	DNP (Note 1)	110	470
1.8	10	47 + 22	90.9	45.5	22	DNP (Note 1)	90	470

Note:
1. Connect FS1 to VCC1.

1.2 Block Diagram

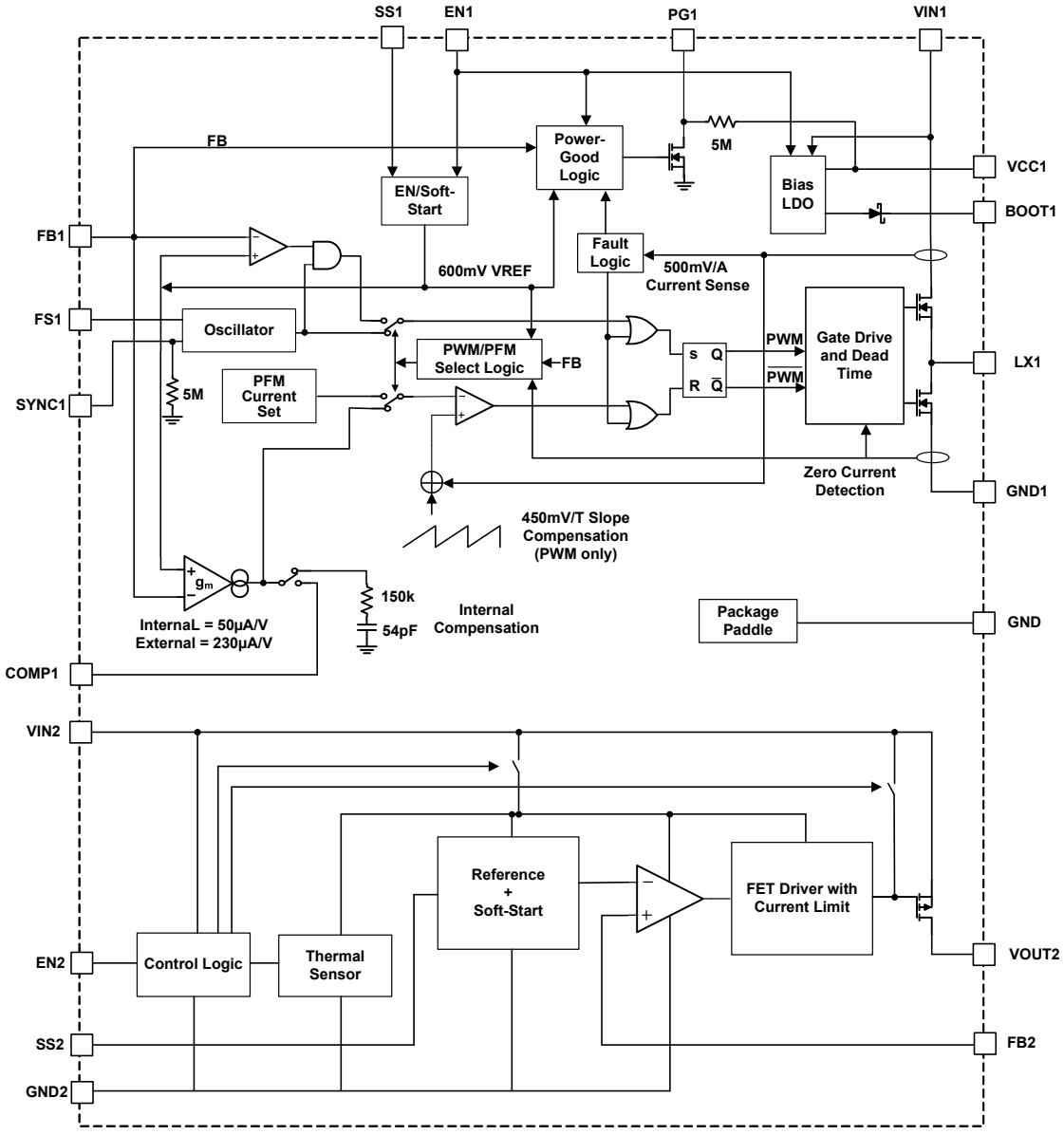


Figure 5. Functional Block Diagram

1.3 Ordering Information

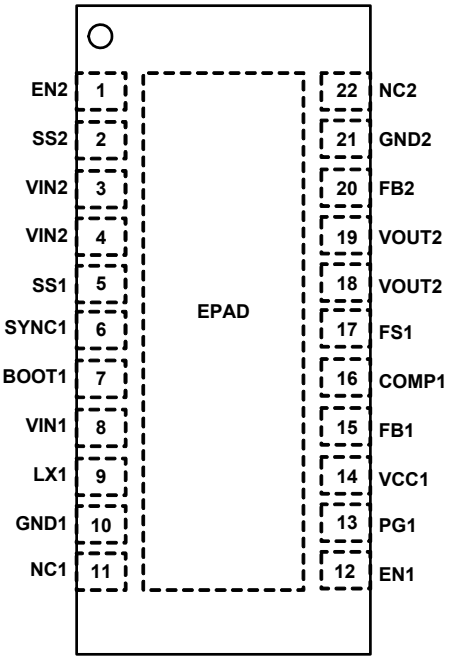
Part Number (Notes 3, 4)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 2)	Package (RoHS Compliant)	Pkg. Dwg. #
RAA2124214GNP#AA0	RAA212421	-40 to +125	-	22 Ld TDFN	L22.3x6
RAA2124214GNP#HA0	RAA212421	-40 to +125	6k	22 Ld TDFN	L22.3x6
RAA2124214GNP#MA0	RAA212421	-40 to +125	250	22 Ld TDFN	L22.3x6

Notes:

2. See TB347 for details about reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the RAA212421 device page. For more information about MSL, see TB363.

1.4 Pin Configurations

22 Ld 3x6 QFN
Top View



1.5 Pin Descriptions

Pin Number	Pin Name	Description
1	EN2	VIN2 independent chip enable. TTL and CMOS compatible.
2	SS2	The external capacitor on this pin adjusts the start-up ramp and controls inrush current.
3, 4	VIN2	Input supply. A minimum of 4.7µF X5R/X7R input capacitor is required for proper operation. See "External Capacitor Requirements (LDO)" on page 30 for more details.
5	SS1	Controls the output soft-start ramp time. A single capacitor from the SS1 pin to ground determines the output ramp rate. See "Soft-Start" on page 20 for soft-start details. If the SS1 pin is tied to VCC1, an internal soft-start of 2ms is used.

Pin Number	Pin Name	Description
6	SYNC1	Synchronization and light-load operational mode selection input. Connect to logic high or VCC for PWM mode. Connect to logic low or ground for PFM mode. Logic ground enables the IC to automatically choose PFM or PWM operation. Connect to an external clock source for synchronization with positive edge trigger. The sync source must be higher than the programmed IC frequency. An internal 5MΩ pull-down resistor prevents an undefined logic state if SYNC is left floating.
7	BOOT1	Floating bootstrap supply pin for the power MOSFET gate driver. The bootstrap capacitor provides the necessary charge to turn on the internal N-channel MOSFET. Connect an external 100nF capacitor from this pin to LX1.
8	VIN1	The input supply for the power stage of the regulator and the source for the internal linear bias regulator. Place a minimum of 4.7µF ceramic capacitance from VIN1 to GND1 and close to the IC for decoupling.
9	LX1	Switch node output. This pin connects the switching FETs with the external output inductor.
10	GND1	Ground connection. Connect directly to the system GND plane.
11, 22	NC1, NC2	No Connect
12	EN1	Regulator enable input. The regulator and bias LDO are held off when the pin is pulled to ground. The chip is enabled when the voltage on this pin rises above 1V. Connect this pin to VIN1 for automatic start-up. Do not connect the EN1 pin to VCC1, because the LDO is controlled by EN1 voltage.
13	PG1	Open-drain, power-good output that is pulled to ground when the output voltage is below regulation limits or during the soft-start interval. There is an internal 5MΩ internal pull-up resistor.
14	VCC1	Output of the internal 5V linear bias regulator. Decouple to GND with a 1µF ceramic capacitor at the pin.
15	FB1	Feedback pin for the regulator. FB1 is the inverting input to the voltage loop error amplifier. COMP1 is the output of the error amplifier. The output voltage is set by an external resistor divider connected to FB1. In addition, the PWM regulator's power-good and UVLO circuits use FB1 to monitor the regulator output voltage.
16	COMP1	COMP1 is the output of the error amplifier. When it is tied to VCC1, internal compensation is used. When only an RC network is connected from COMP1 to GND, external compensation is used. See "Loop Compensation Design" on page 27 for more details.
17	FS1	Frequency selection pin. Tie to VCC1 for the 500kHz switching frequency. Connect a resistor to GND1 for an adjustable frequency from 300kHz to 2MHz.
18, 19	VOUT2	Regulated LDO output voltage. A minimum 4.7µF X5R/X7R output capacitor is required for stability. See "External Capacitor Requirements (LDO)" on page 30 for more details.
20	FB2	The input to the control loop error amplifier. It sets the LDO output voltage.
21	GND2	LDO ground.
EPAD	GND	Ground connection. Connect to application board GND plane with at least five vias. All voltage levels are measured with respect to this pin. The EPAD must not float.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VIN1 to GND	-0.3	+43	V
LX1 to GND (DC)	-0.3	VIN1 + 0.3	V
LX1 to GND (20ns)	-2	+44	V
EN1 to GND	-0.3	+43	V
BOOT1 to LX1	-0.3	+5.5	V
COMP1, FS1, PG1, SYNC1, SS1, VCC1 to GND	-0.3	+5.9	V
FB1 to GND	-0.3	+2.95	V
VIN2 to GND	-0.3	+6.5	V
VOUT2 to GND (DC)	-0.3	+6.5	V
EN2, FB2, SS2 to GND	-0.3	+6.5	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2014)	2		kV
Charged Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
22 Ld 6x3 QFN Package (Notes 5, 6)	32	3.3

Notes:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Ambient Temperature Range	-40	+125	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{IN1}	3	40	V
Supply Voltage, V_{IN2}	1.8	6	V
Ambient Temperature	-40	+125	°C
Output Voltage, V_{OUT2}	0.8	5.5	V

2.4 Electrical Specifications

Recommended operating conditions, V_{CC1} = 3.3V, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
Buck Regulator						
Supply Voltage						
V_{IN1} Voltage Range	V_{IN1}		3		40	V
V_{IN1} Quiescent Supply Current	I_{Q1}	SYNC1 = 5V, $f_{SW} = V_{CC1}$		8		mA
V_{IN1} Shutdown Supply Current	I_{SD1}	EN1 = 0V, V_{IN1} = 40V (Note 7)		2	4	µA
V_{CC1} Voltage	V_{CC1}	V_{IN1} = 6V, I_{OUT} = 0 to 10mA	4.5	5.1	5.7	V
Power-On Reset						
V_{CC1} POR Threshold		Rising edge		2.75	2.95	V
		Falling edge	2.35	2.6		V
Oscillator						
Nominal Switching Frequency	f_{SW}	FS1 pin = V_{CC1}	430	500	570	kHz
		Resistor from FS1 pin to GND1 = 340kΩ	240	300	360	kHz
		Resistor from FS1 pin to GND1 = 32.4kΩ		2000		kHz
Minimum Off-Time	t_{OFF}	V_{IN1} = 3V		150		ns
Minimum On-Time	t_{ON}	(Note 10)		90		ns
FS1 Voltage	V_{FS}	R_{FS1} = 100kΩ	0.39	0.4	0.41	V
Synchronization Frequency	SYNC1		300		2000	kHz
SYNC Pulse Width			100			ns
Error Amplifier						
Error Amplifier Transconductance Gain	g_{m1}	External compensation	165	230	295	µA/V
		Internal compensation		50		µA/V
FB1 Leakage Current		V_{FB1} = 0.6V		1	150	nA
Current Sense Amplifier Gain	R_{T1}		0.44	0.5	0.54	V/A
FB1 Voltage		T_A = -40°C to +85°C	0.590	0.599	0.606	V
		T_A = -40°C to +125°C	0.590	0.599	0.607	V
Power-Good						
Lower PG1 Threshold - VFB1 Rising				90	94	%
Lower PG1 Threshold - VFB1 Falling			82.5	86		%
Upper PG1 Threshold - VFB1 Rising				116.5	120	%
Upper PG1 Threshold - VFB1 Falling			107	112		%
PG1 Propagation Delay		Percentage of the soft-start time		10		%
PG1 Low Voltage		I_{SINK} = 3mA, EN1 = V_{CC1}, VFB1 = 0V		0.05	0.3	V
Tracking and Soft-Start (SS1)						
Soft-Start Charging Current	I_{SS1}		4.2	5.5	6.7	µA
Internal Soft-Start Ramp Time		EN1/SS1 = V_{CC1}	1.5	2.4	3.4	ms

Recommended operating conditions, V_{CC1} = 3.3V, unless otherwise specified. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
Fault Protection						
Thermal Shutdown Temperature	T_{SD}	Rising threshold		150		°C
	T_{HYS}	Hysteresis		25		°C
Current Limit Blanking Time	t_{OCON}			17		Clock pulses
Overcurrent and Auto Restart Period	t_{OCOFF}			8		SS cycle
Positive Peak Current Limit	I_{PLIMIT}	(Note 8)	1.3	1.6	1.8	A
PFM Peak Current Limit	I_{PK_PFM}		0.34	0.4	0.5	A
Zero Cross Threshold				15		mA
Negative Current Limit	I_{NLIMIT}	(Note 8)	-0.68	-0.6	-0.53	A
Power MOSFET						
High-Side	R_{HDS}	I_{PHASE} = 100mA, V_{CC1} = 5V		313		mΩ
Low-Side	R_{LDS}	I_{PHASE} = 100mA, V_{CC1} = 5V		175		mΩ
LX1 Leakage Current		EN1 = LX1 = 0V			300	nA
LX1 Rise Time	t_{RISE}	V_{IN1} = 40V		10		ns
EN1/SYNC1						
Input Threshold		Falling edge, logic low	0.4	1		V
		Rising edge, logic high		1.2	1.4	V
EN1 Logic Input Leakage Current		EN1 = 0V/40V	-0.65		0.65	µA
SYNC1 Logic Input Leakage Current		SYNC1 = 0V		10	100	nA
		SYNC1 = 5V		1.0	1.55	µA
LDO Regulator						
DC Characteristics						
Input Voltage	V_{IN2}	0°C < T_J < +125°C	1.8		6.0	V
		-40°C < T_J < +125°C	2.2		6.0	V
Feedback Pin Voltage	V_{FB2}	1.8V < V_{IN2} < 6V; 0A < I_{LOAD2} < 500mA	491	500	509	mV
Feedback Input Current		V_{FB2} = 0.5V		0.01	1	µA
Line Regulation	($V_{OUT2(LOW\ LINE)}$ - $V_{OUT2(HIGH\ LINE)}$)/ $V_{OUT2(LOW\ LINE)}$	V_{IN2} = 1.8V to 6V; I_{LOAD2} = 100mA	-0.9		0.9	%
Load Regulation	($V_{OUT2(NO\ LOAD)}$ - $V_{OUT2(FULL\ LOAD)}$)/ $V_{OUT2(NO\ LOAD)}$	V_{IN2} = 2.2V; I_{LOAD2} = 0A to 500mA	-0.7		0.7	%
Ground Pin Current	I_{Q2}	I_{LOAD2} = 0A, 1.8V < V_{IN2} < 6V		2.2	4.6	mA
		I_{LOAD2} = 500mA, 1.8V < V_{IN2} < 6V		2.8	5.7	mA
Ground Pin Current in Shutdown	I_{SHDN}	EN2 pin = 0V, V_{IN2} = 6V		0.2	12	µA
Dropout Voltage (Note 11)	V_{DO}	I_{LOAD2} = 500mA, V_{OUT2} = 2.5V		45	90	mV
Output Short-Circuit Current	OCP	V_{OUT2} = 0V	0.75	1.2	1.5	A
Thermal Shutdown Temperature	TSD			160		°C

Recommended operating conditions, V_{CC1} = 3.3V, unless otherwise specified. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
Thermal Shutdown Hysteresis	TSDn	V_{IN2} = 3.3V		10		°C
AC Characteristics						
Input Supply Ripple Rejection	PSRR	f = 1kHz, I_{LOAD2} = 500mA; V_{IN2} = 2.2V; V_{OUT} = 1.8V		57		dB
		f = 120Hz, I_{LOAD2} = 500mA; V_{IN2} = 2.2V; V_{OUT2} = 1.8V		60		dB
Output Noise Voltage		V_{IN2} = 2.2V; V_{OUT2} = 1.8V; I_{LOAD2} = 500mA, BW = 100Hz < f < 100kHz		79		μV_{RMS}
Enable (EN2) Pin Characteristics						
Turn-On Threshold			0.5	0.8	1	V
Hysteresis			10	80	200	mV
EN2 Pin Turn-On Delay		C_{OUT2} = 4.7µF, I_{LOAD2} = 500mA		100		µs
EN2 Pin Leakage Current		V_{IN2} = 6V, EN2 = 3V			1	µA
Soft-Start (SS2) Characteristics						
SS2 Pin Currents (Note 12)	I_{PD}	V_{IN2} = 3.5V, EN2 = 0V, SS2 = 1V	0.5	1	1.3	mA
	I_{CHG}		-3.3	-2	-0.8	µA

Notes:

7. Test Condition: V_{IN1} = 40V, FB1 forced above regulation point (0.6V), no switching, and power MOSFET gate charging current not included.
8. Established by both current sense amplifier gain test and current sense amplifier output test at I_L = 0A.
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. Minimum on-time required to maintain loop stability.
11. Dropout is defined as the difference in supply V_{IN} and V_{OUT} when the output is below its nominal regulation.
12. I_{PD} is the internal pull-down current that discharges the external SS2 capacitor on disable. I_{CHG} is the current from the SS2 pin that charges the external soft start capacitor during start-up.

3. Typical Performance Curves

3.1 Buck Efficiency Curves

f_{SW} = 500kHz, T_A = +25°C

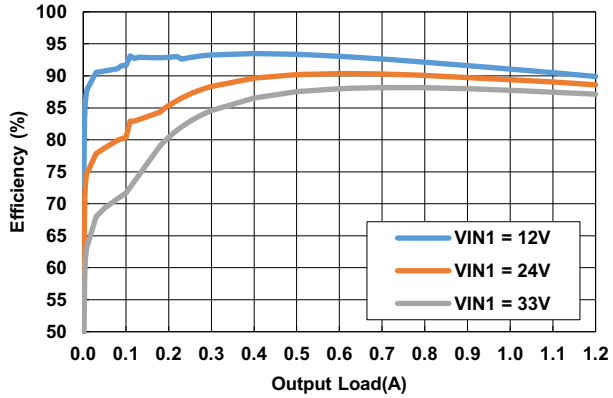


Figure 6. Efficiency vs Load, PFM, V_{OUT} = 5V, L_1 = 22µH

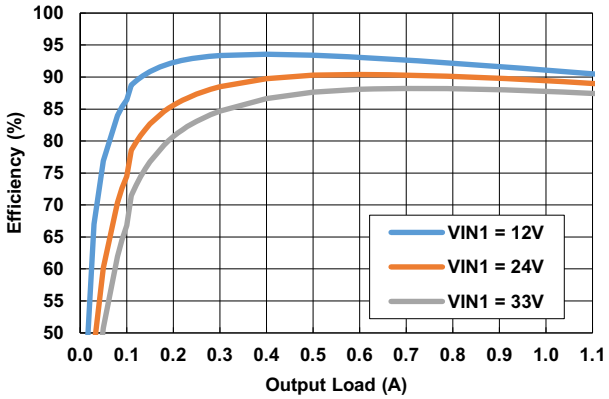


Figure 7. Efficiency vs Load, PWM, V_{OUT1} = 5V, L_1 = 22µH

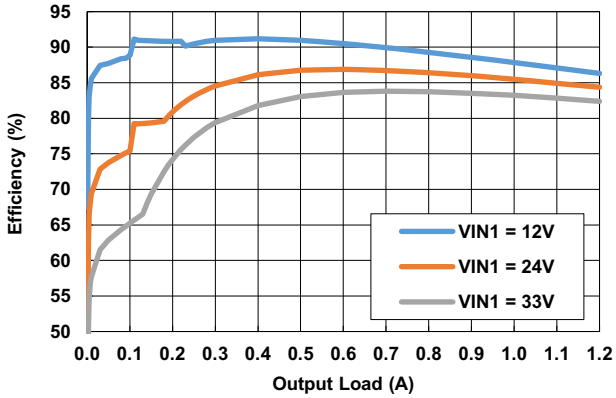


Figure 8. Efficiency vs Load, PFM, V_{OUT} = 3.3V, L_1 = 22µH

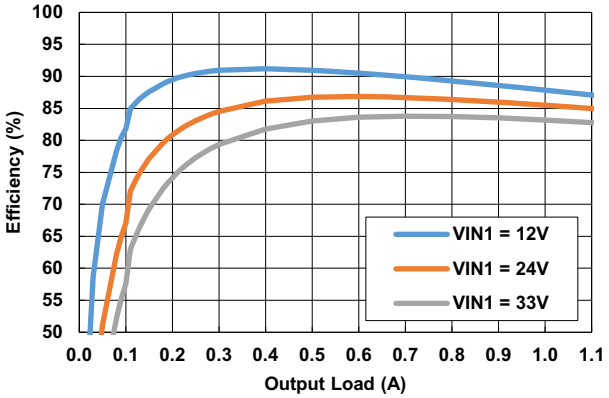


Figure 9. Efficiency vs Load, PWM, V_{OUT1} = 3.3V, L_1 = 22µH

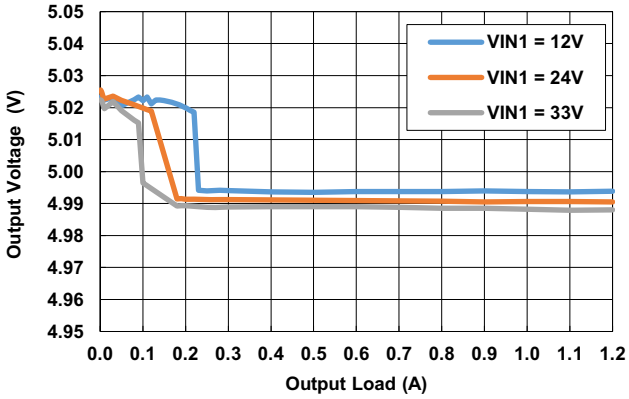


Figure 10. V_{OUT} Regulation vs Load, PFM, V_{OUT1} = 5V

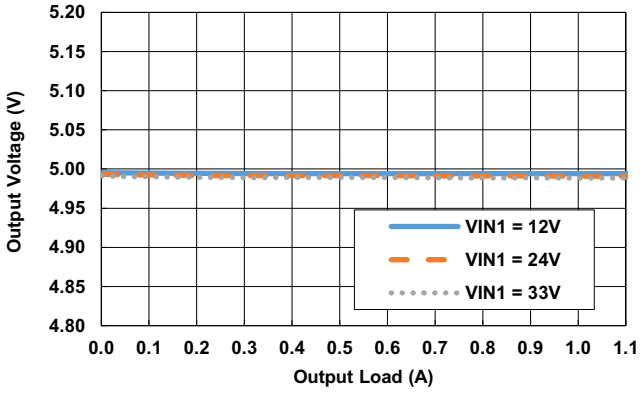


Figure 11. V_{OUT1} Regulation vs Load, PWM, V_{OUT1} = 5V

f_{SW} = 500kHz, T_A = +25°C

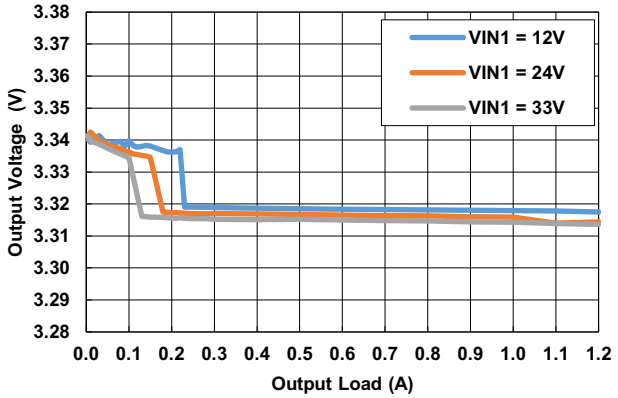


Figure 12. V_{OUT} Regulation vs Load, PFM, V_{OUT1} = 3.3V

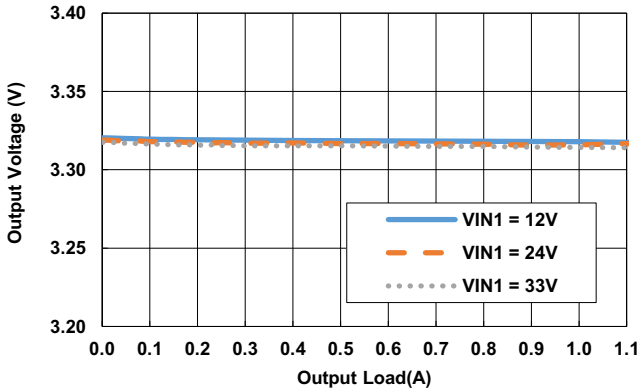


Figure 13. V_{OUT1} Regulation vs Load, PWM, V_{OUT1} = 3.3V

3.2 Buck Measurements

f_{SW} = 500kHz, V_{IN1} = 24V, V_{OUT1} = 3.3V, T_A = +25°C

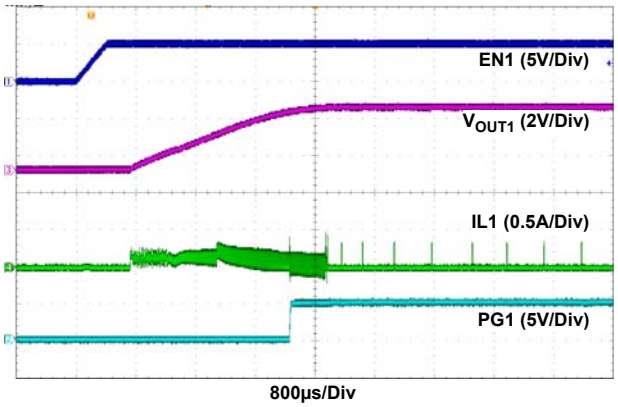


Figure 14. Start-Up at No Load, PFM

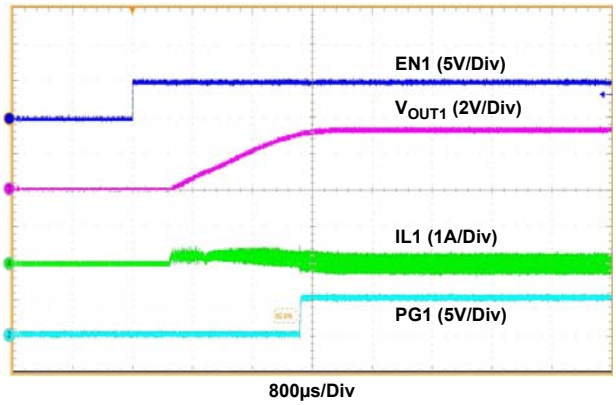


Figure 15. Start-Up at No Load, PWM

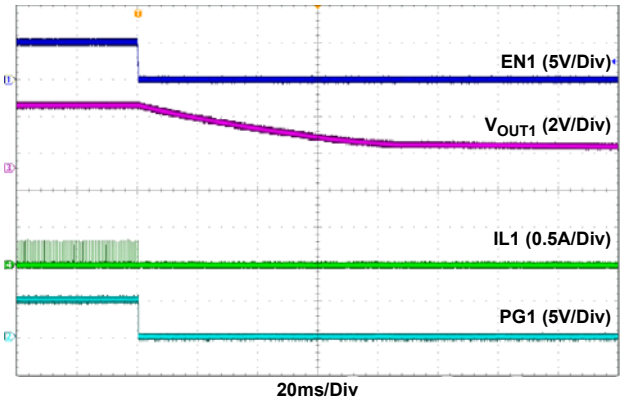


Figure 16. Shutdown at No Load, PFM

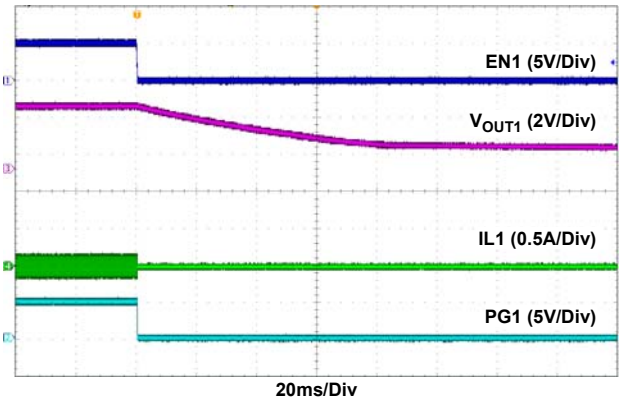


Figure 17. Shutdown at No Load, PWM

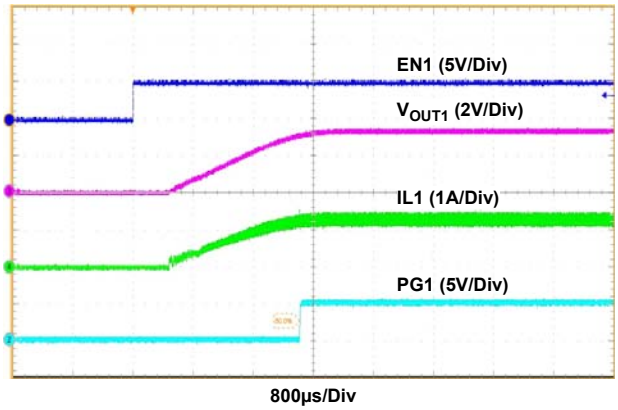


Figure 18. Start-Up at 1.1A, PWM

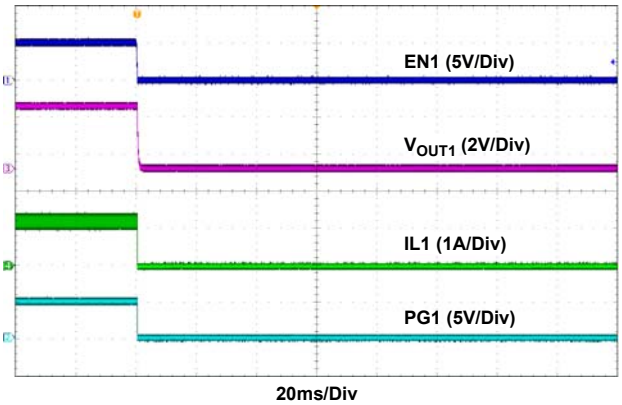


Figure 19. Shutdown at 1.1A, PWM

f_{SW} = 500kHz, V_{IN1} = 24V, V_{OUT1} = 3.3V, T_A = +25°C **(Continued)**

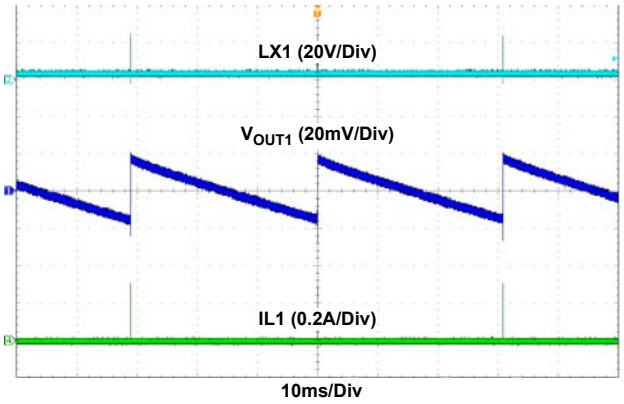


Figure 20. Steady State at No Load, PFM

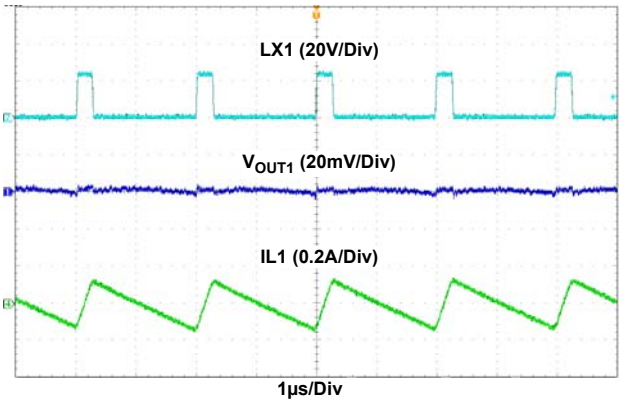


Figure 21. Steady State at No Load, PWM

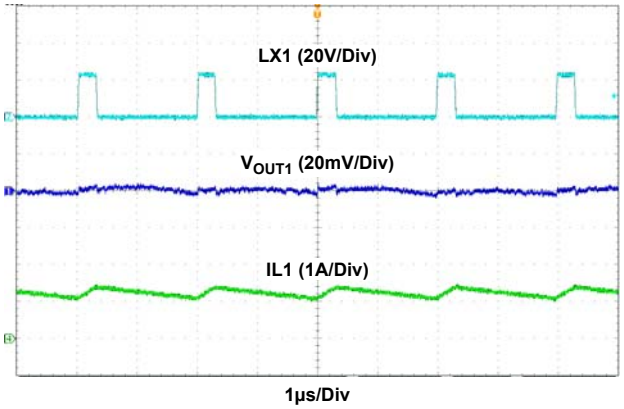


Figure 22. Steady State at 1.1A Load

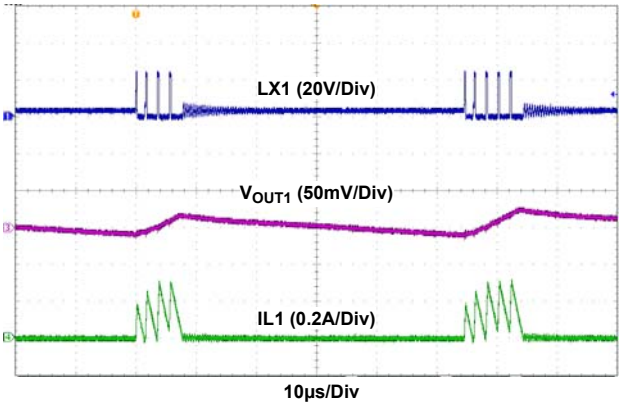


Figure 23. Light Load Operation at 20mA, PFM

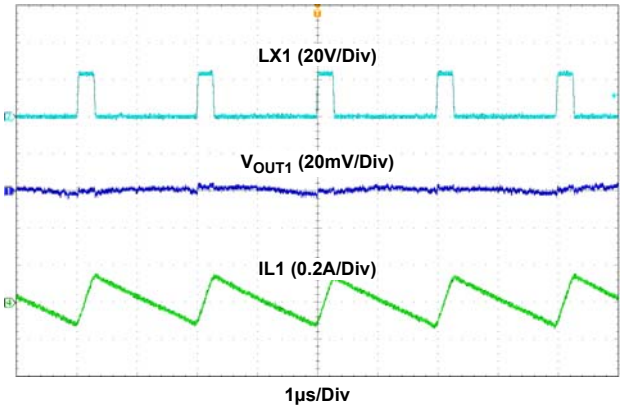


Figure 24. Light Load Operation at 20mA, PWM

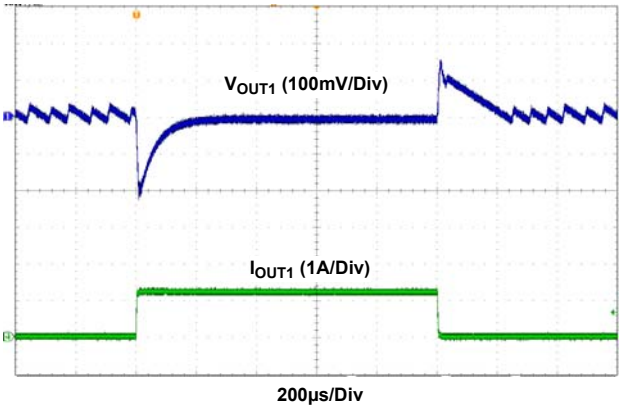


Figure 25. Load Transient, PFM

f_{SW} = 500kHz, V_{IN1} = 24V, V_{OUT1} = 3.3V, T_A = +25°C **(Continued)**

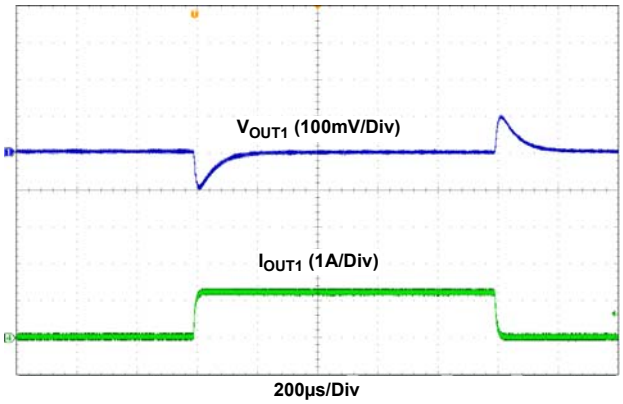


Figure 26. Load Transient, PWM

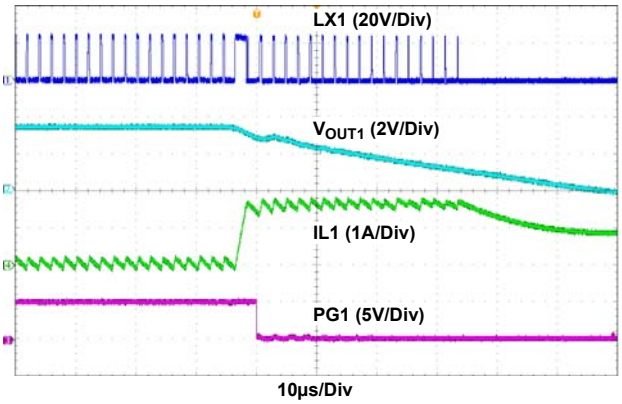


Figure 27. Overcurrent Protection

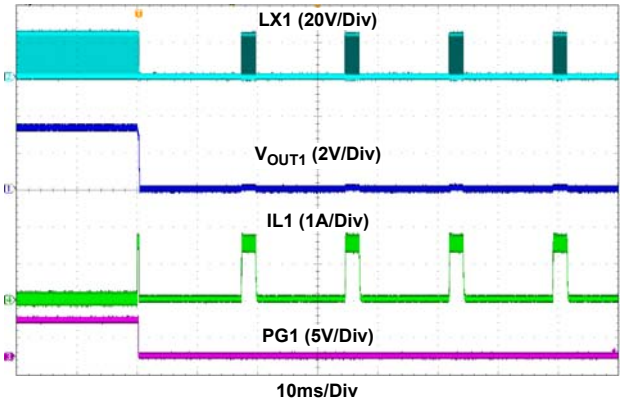


Figure 28. Overcurrent Protection Hiccup

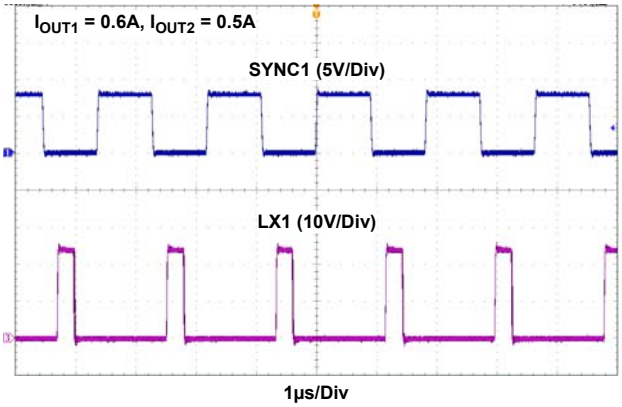


Figure 29. SYNC1 at 1.1A Load

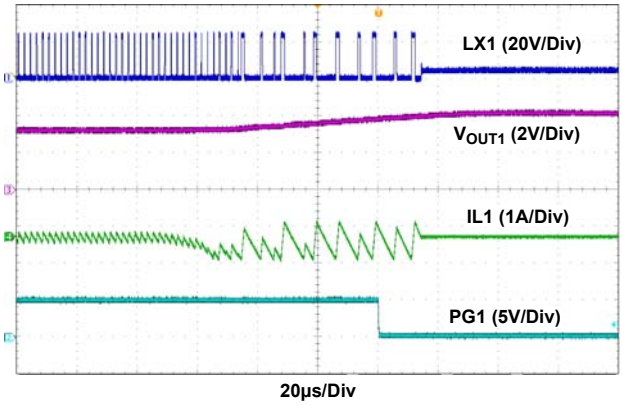


Figure 30. Negative Current Limit

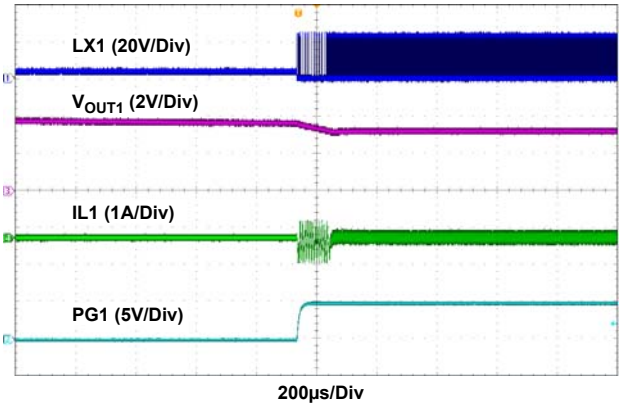


Figure 31. Negative Current Limit Recovery

3.3 LDO Characteristics

Unless otherwise noted: V_{IN2} = 2.2V, V_{OUT2} = 1.8V, C_{IN2} = C_{OUT2} = 10µF, T_J = +25°C, I_{LOAD} = 0A

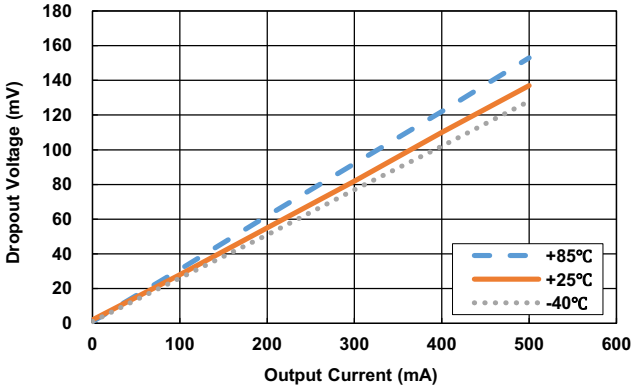


Figure 32. Dropout vs Output Current

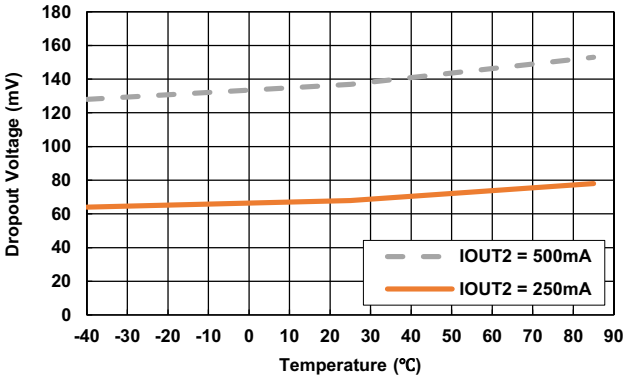


Figure 33. Dropout vs Temperature

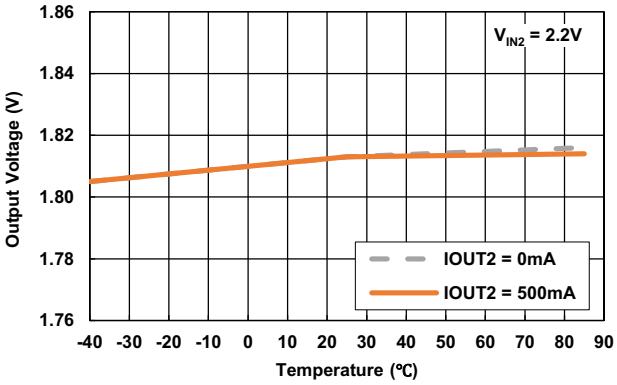


Figure 34. Output Voltage vs Temperature

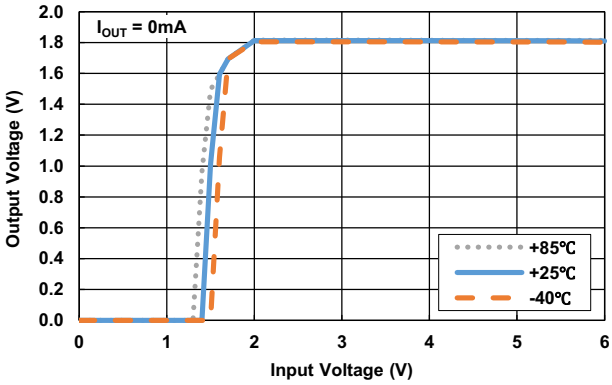


Figure 35. Output Voltage vs Input Voltage

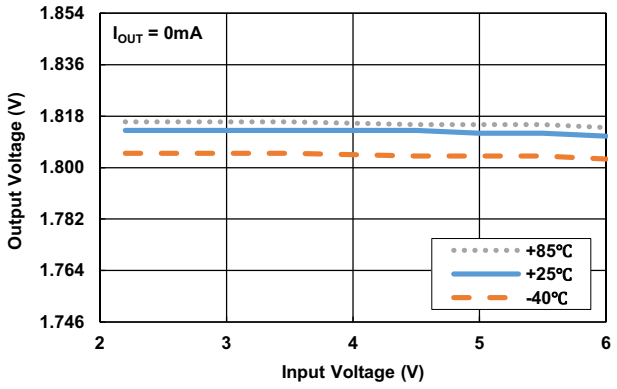


Figure 36. Line Regulation

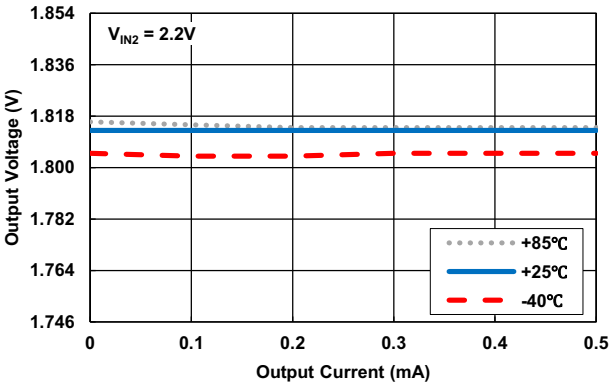


Figure 37. Output Voltage vs Output Current

Unless otherwise noted: V_{IN2} = 2.2V, V_{OUT2} = 1.8V, C_{IN2} = C_{OUT2} = 10µF, T_J = +25°C, I_{LOAD} = 0A **(Continued)**

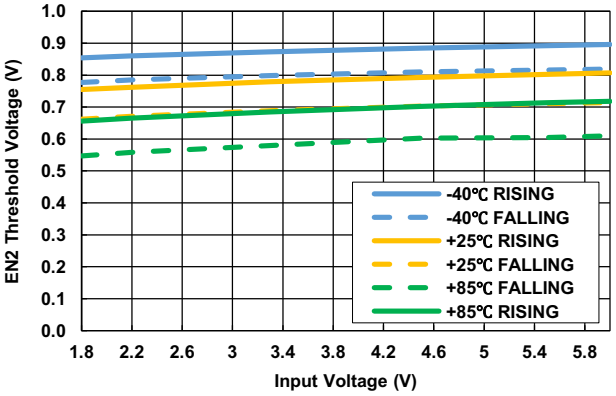


Figure 38. EN2 Thresholds vs Input Voltage

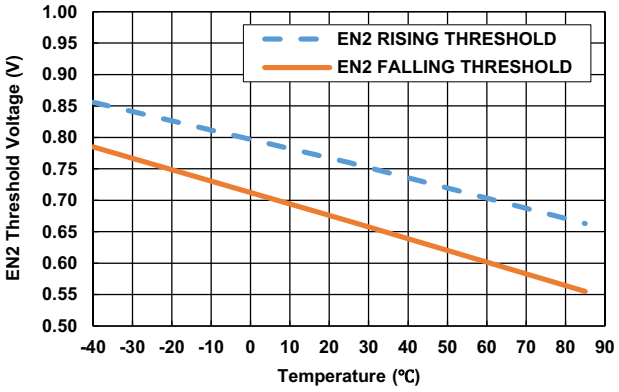


Figure 39. EN2 Thresholds vs Temperature

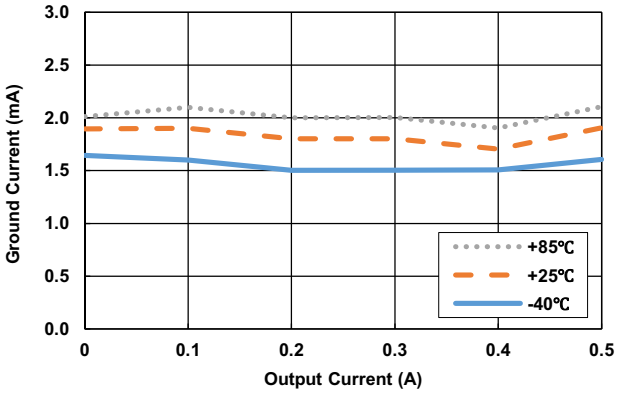


Figure 40. Ground Current vs Output Current

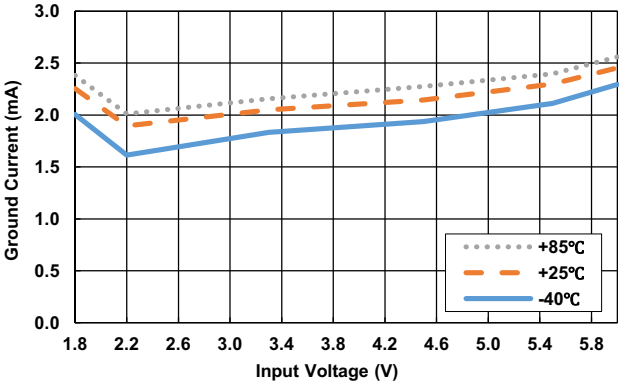


Figure 41. Ground Current vs Input Voltage

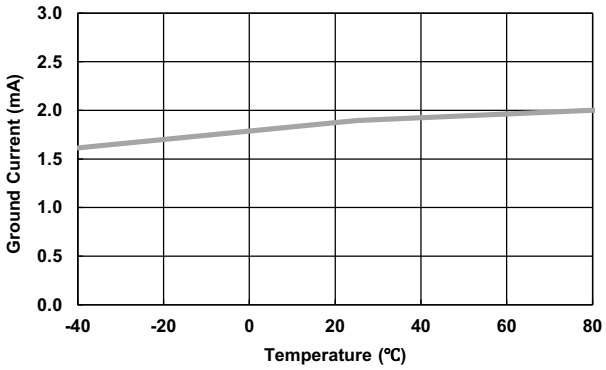


Figure 42. Ground Current vs Temperature

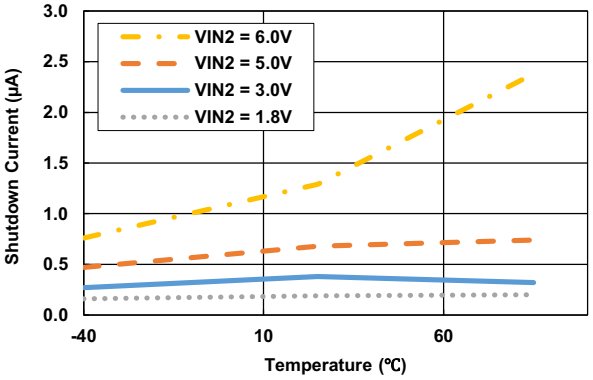


Figure 43. Shutdown Current vs Temperature

Unless otherwise noted: V_{IN2} = 2.2V, V_{OUT2} = 1.8V, C_{IN2} = C_{OUT2} = 10µF, T_J = +25°C, I_{LOAD} = 0A **(Continued)**

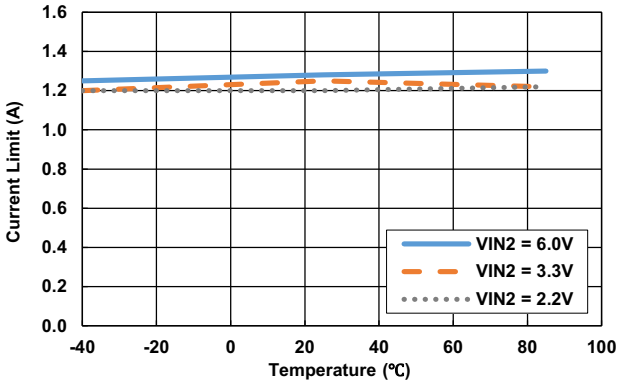


Figure 44. Current Limit vs Temperature

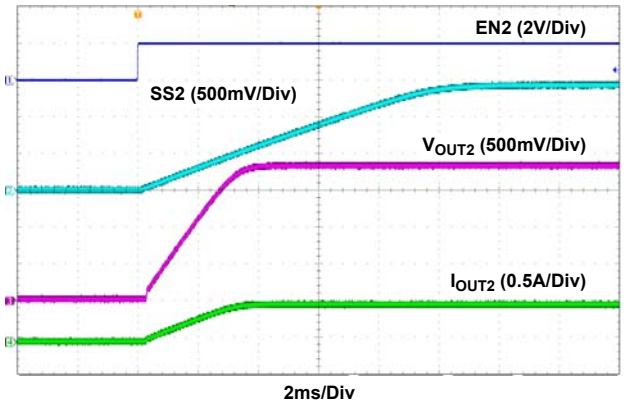


Figure 45. Enable Start-Up (C_{SS2} = 10nF)

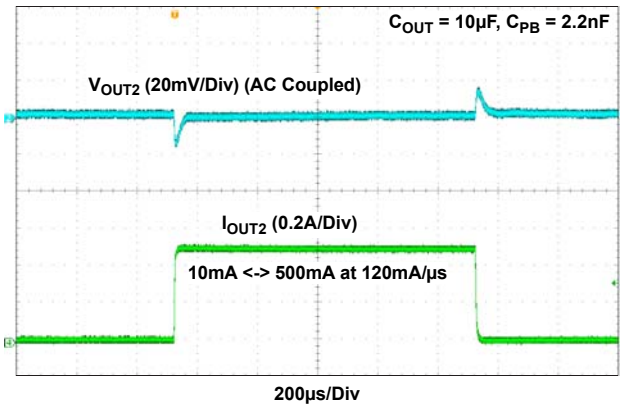


Figure 46. Load Transient Response

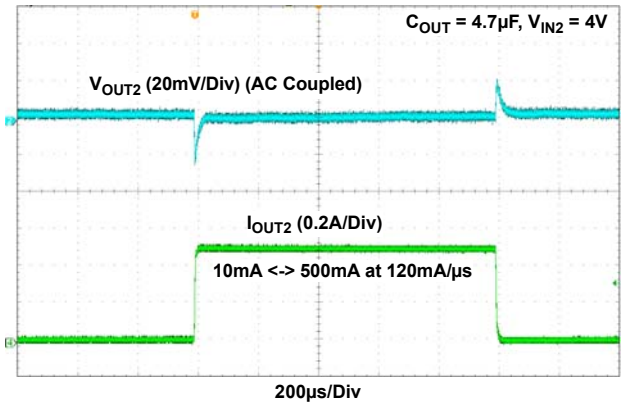


Figure 47. Load Transient Response

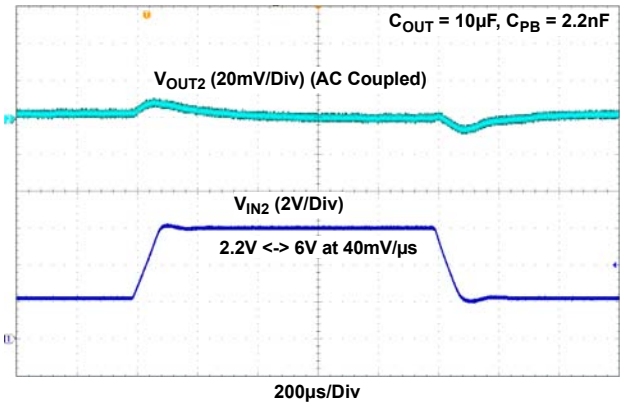


Figure 48. Line Transient Response

Unless otherwise noted: V_{IN2} = 2.2V, V_{OUT2} = 1.8V, C_{IN2} = C_{OUT2} = 10µF, T_J = +25°C, I_{LOAD} = 0A **(Continued)**

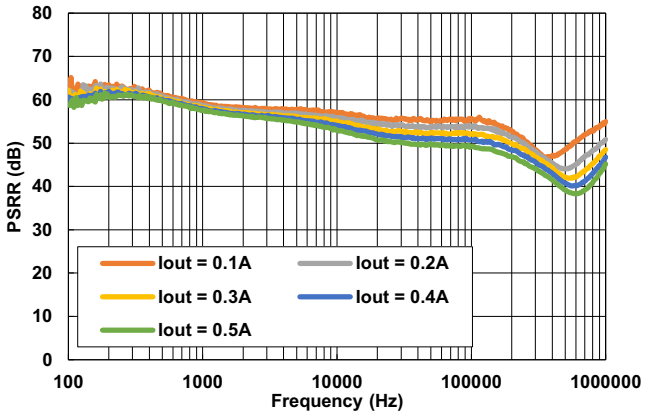


Figure 49. PSRR vs Frequency, C_{PB} = 10nF

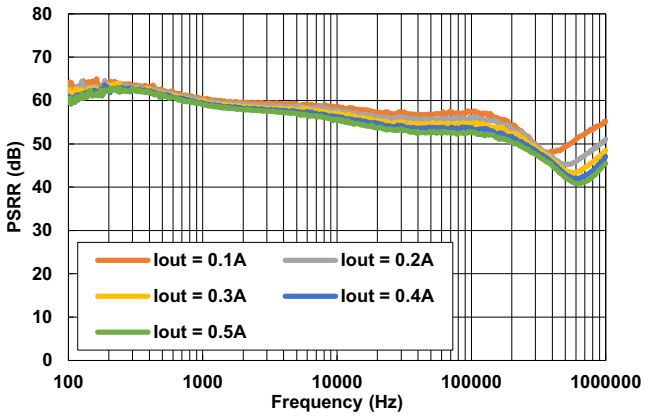


Figure 50. PSRR vs Frequency, C_{PB} = 10nF, V_{IN} = 2.3V

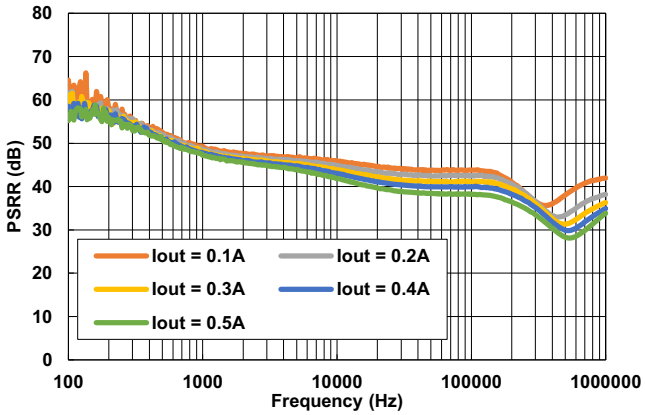


Figure 51. PSRR vs Frequency (C_{OUT} = 4.7µF)

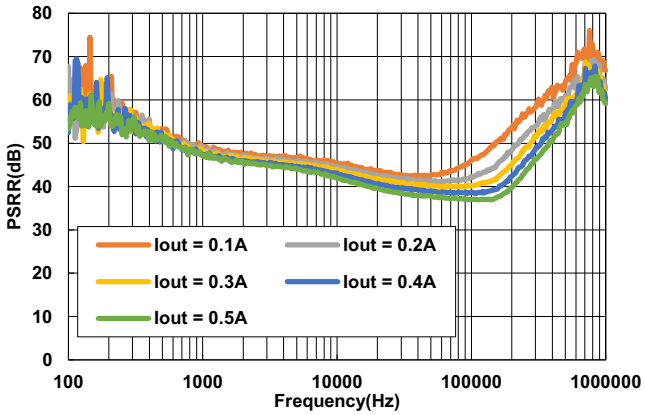


Figure 52. PSRR vs Frequency (C_{OUT} = 47µF)

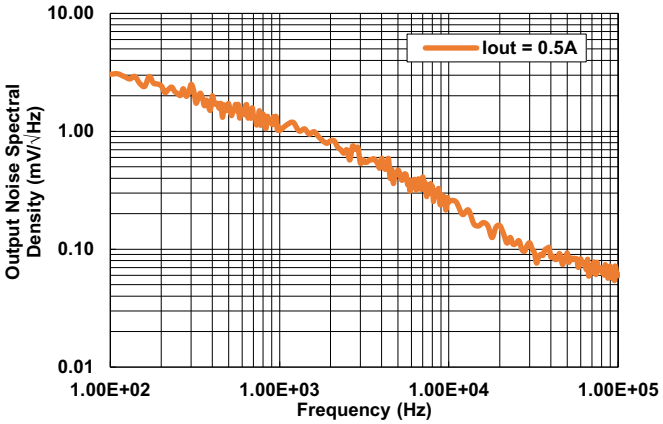


Figure 53. Output Noise Spectral Density

4. Functional Description

The RAA212421 consists of a constant frequency current mode wide V_{IN} buck regulator and a low dropout regulator (LDO). The wide V_{IN} buck regulator can operate from an unregulated DC source, such as a battery, with a voltage ranging from +3V to +40V. An internal linear regulator provides bias to the low voltage portions of the wide V_{IN} buck regulator. Peak current mode control simplifies feedback loop compensation and rejects input voltage variation. User selectable internal feedback loop compensation further simplifies design. The buck regulator is equipped with an internal current sensing circuit, and the peak current limit threshold is typically set at 1.6A.

The low dropout regulator operates from 1.8V to 6V input voltage and regulates the output voltage between 0.8V to 5.5V with a maximum output current of 500mA. This product family uses a submicron BiCMOS process for the best in class analog performance and overall value. This CMOS LDO consumes significantly lower quiescent current as a function of load compared to bipolar LDOs, which translates into higher frequency efficiency and packages with smaller footprints.

4.1 Power-On Reset (Buck)

The wide V_{IN} buck regulator automatically initializes upon receipt of the input power supply and continually monitors the EN1 pin state. If EN1 is held below its logic rising threshold, the IC is held in shutdown and consumes typically 2µA from the V_{IN1} supply. If EN1 exceeds its logic rising threshold, the regulator enables the bias linear regulator and begins to monitor the VCC1 pin voltage. When the VCC1 pin voltage passes its rising POR threshold, the controller initializes the switching regulator circuits. If V_{CC1} never passes the rising POR threshold, the controller prevents the switching regulator from operating. If V_{CC1} falls below its falling POR threshold while the switching regulator is operating, the switching regulator is shut down until V_{CC1} returns.

4.2 Soft-Start

Both the buck converter and the LDO have a soft-start feature to avoid large inrush current. For the buck converter, V_{OUT1} is slowly increased at startup to its final regulated value. Soft-start time is determined by the SS1 pin connection. If the SS1 is pulled to VCC1, an internal 2ms timer is selected for soft-start. For other soft-start times, connect a capacitor from SS1 to GND. In this case, a 5.5µA current pulls up the SS1 voltage, and the FB1 pin follows this ramp until it reaches the 600mV reference level. The soft-start time for this case is described by Equation 1:

(EQ. 1) $$Time(ms) = C(nF)*0.109$$

The soft-start circuit of the LDO controls the rate at which the output voltage rises up to regulation at power-up or LDO enable. This start-up ramp time can be set by adding an external capacitor from the SS2 pin to ground. An internal 2µA current source charges up the C_{SS2}, and the feedback reference voltage is clamped to the voltage across it. The start-up time is set by Equation 2.

(EQ. 2) $$t_{start} = \frac{C_{SS2} x 0.5}{2\mu A}$$

Equation 3 determines the C_{SS2} required for a specific start-up inrush current where V_{OUT2} is the output voltage, C_{OUT2} is the total capacitance on the output, and $I_{INRUSH2}$ is the desired inrush current.

(EQ. 3) $$C_{SS2} = \frac{V_{OUT2} x C_{OUT2} x 2\mu A}{I_{INRUSH2} x 0.5V}$$

The external capacitor is always discharged to ground at the beginning of start-up or enable.

4.3 Power-Good (Buck)

PG1 is the open-drain output of a window comparator that continuously monitors the buck regulator output voltage with the FB1 pin. PG1 is actively held low when EN1 is low and during the buck regulator soft-start period. After the soft-start period completes, PG1 becomes high impedance if the FB1 pin is within the range specified in the "Electrical Specifications" on page 8. If FB1 exits the specified window, PG1 is pulled low until FB1 returns.

Over-temperature faults also force PG1 low until the fault condition is cleared by an attempt to soft-start. PG1 has an internal 5MΩ pull-up resistor.

4.4 PWM Control Scheme (Buck)

The wide V_{IN} buck regulator employs peak current-mode Pulse-Width Modulation (PWM) control for fast transient response and pulse-by-pulse current limiting as shown in the "Functional Block Diagram" on page 4. The current loop consists of the current sensing circuit, slope compensation ramp, PWM comparator, oscillator, and latch. Current sense trans-resistance is typically 500mV/A and the slope compensation rate, Se, is typically 450mV/T where T is the switching cycle period. The control reference for the current loop comes from the error amplifier's output (V_{COMP1}).

A PWM cycle begins when a clock pulse sets the PWM latch and the upper FET is turned on. Current begins to ramp up in the upper FET and inductor. This current is sensed, converted to a voltage (V_{CSA}), and summed with the slope compensation signal. This combined signal is compared to V_{COMP1}, and the latch is reset when the signal is equal to V_{COMP1}. Upon latch reset, the upper FET is turned off and the lower FET is turned on allowing the current to ramp down in the inductor. The lower FET remains on until the clock initiates another PWM cycle. Figure 54 shows the typical operating waveforms during PWM operation. The dotted lines illustrate the sum of the current sense and slope compensation signal.

The output voltage is regulated as the error amplifier varies V_{COMP1} with changes to the output inductor current. The error amplifier is a transconductance type, and its output (COMP1) is terminated with a series RC network to GND. This termination is internal (150k/54pF) if the COMP1 pin is tied to VCC1. In addition, the transconductance for COMP1 = V_{CC1} is 50µA/V versus 230µA/V for external RC connection. The non-inverting input of the error amplifier is internally connected to a 600mV reference voltage, and its inverting input is connected to the output voltage from the FB1 pin and its associated divider network.

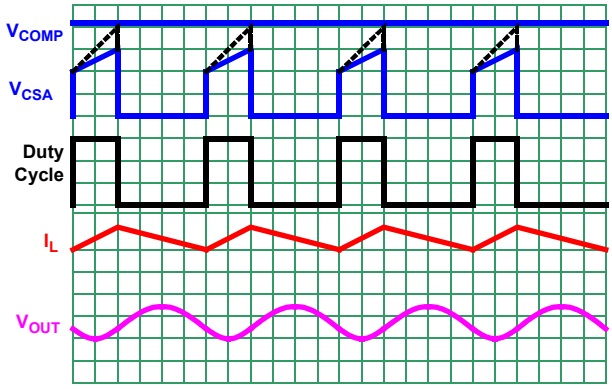


Figure 54. PWM Operation Waveforms

4.5 Light Load Operation

At light loads, converter efficiency can be improved by enabling Pulsed Frequency Modulation (PFM). Connecting the SYNC pin to GND allows the controller to choose PFM operation automatically when the load current is low. Figure 55 on page 22 shows the DCM operation. The IC enters the DCM mode of operation when eight consecutive cycles of inductor current crossing zero are detected. This corresponds to a load current equal to 1/2 the peak-to-peak inductor ripple current and set by Equation 4:

$$I_{OUT} = \frac{V_{OUT}(1-D)}{2Lf_{SW}} \quad \text{(EQ. 4)}$$

where D = duty cycle, f_{SW}= switching frequency, L = inductor value, I_{OUT} = output loading current, and V_{OUT} = output voltage.

While operating in PFM mode, the regulator controls the output voltage with a simple comparator and pulsed FET current. A comparator signals the point at which FB is equal to the 600mV reference at which time the regulator begins providing pulses of current until FB is moved above the 600mV reference by 1%. The current pulses are

approximately 400mA and are issued at a frequency equal to the converter's programmed PWM operating frequency.

Due to the pulsed current nature of PFM mode, the converter can supply limited current to the load. If the load current rises beyond the limit, V_{OUT} begins to decline. A second comparator signals an FB voltage 2% lower than the 600mV reference and forces the converter to return to PWM operation.

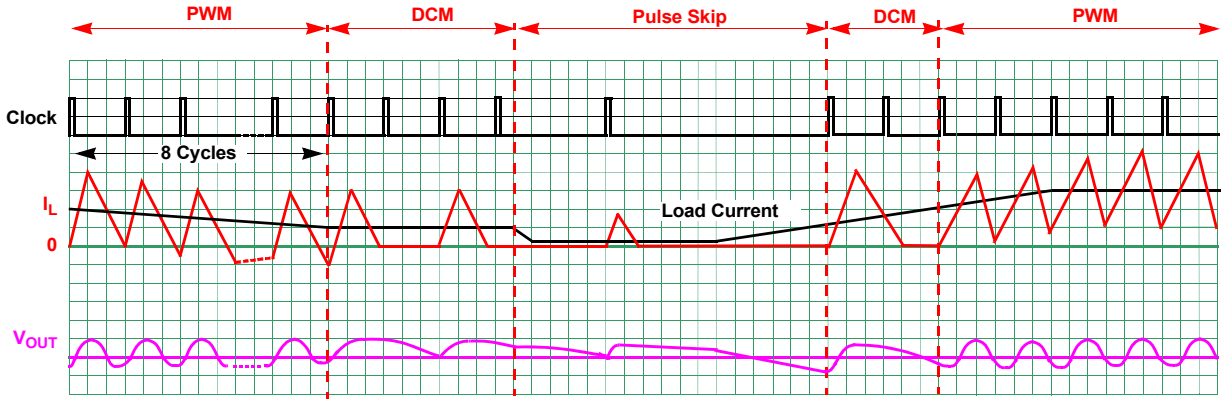


Figure 55. DCM Mode Operation Waveforms

4.6 Output Voltage Selection

The regulator output voltage is easily programmed using an external resistor divider to scale V_{OUT1} relative to the internal reference voltage. The scaled voltage is applied to the inverting input of the error amplifier. See Figure 56 for more information.

The output voltage programming resistor, R_2, depends on both the value chosen for the feedback resistor, R_1, and the regulator's desired output voltage, V_{OUT1}. Equation 5 describes the relationship between V_{OUT1} and resistor values.

$$R_2 = \frac{R_1 \times 0.6V}{V_{OUT1} - 0.6V} \quad \text{(EQ. 5)}$$

If the desired output voltage is 0.6V, R_2 is left unpopulated and R_1 is 0Ω.

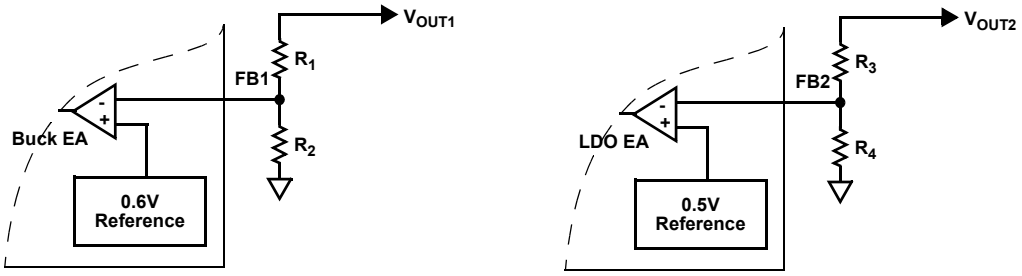


Figure 56. External Resistor Divider

Similarly, the output voltage of the LDO can be set by an external resistor divider network. The values of resistors R_3 and R_4 can be calculated by using Equation 6.

$$R_3 = R_4 \times \left(\frac{V_{OUT2}}{0.5} - 1\right) \quad \text{(EQ. 6)}$$

4.7 Protection Features

The RAA212421 is protected from overcurrent, negative overcurrent, over-temperature, and boot undervoltage. The protection circuits operate automatically.

4.7.1 Overcurrent Protection (Buck)

During PWM on-time, the current through the upper FET is monitored and compared to a nominal 1.6A peak overcurrent limit. If the current reaches the limit, the upper FET is turned off until the next switching cycle. In this way, FET peak current is always well limited.

If the overcurrent condition persists for typically 17 sequential clock cycles, the regulator begins its hiccup sequence. In this case, both FETs are turned off and PG1 is pulled low. This condition is maintained for 8 soft-start periods after which the regulator attempts a normal soft-start.

If the output fault persists, the regulator repeats the hiccup sequence indefinitely. There is no danger even if the output is shorted during soft-start.

If V_{OUT1} is shorted very quickly, FB1 may collapse below 5/8 of its target value before the typical 17 cycles of overcurrent are detected. The RAA212421 recognizes this condition and begins to lower its switching frequency proportional to the FB1 pin voltage. The lowering of the switching frequency ensures that the inductor current does not run away under any circumstances (even with V_{OUT1} near 0V).

4.7.2 Current Limit Protection (LDO)

The RAA212421 LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The LDO performs as a constant current source when the output current exceeds the current limit threshold noted in the Electrical Specifications on page 9. If the short or overload condition is removed from VOUT2, the output returns to normal voltage regulation mode. In the event of an overload condition, the LDO may begin to cycle on and off due to the die temperature exceeding thermal fault condition. The LDO may subsequently begin cooling down after the power device is turned off.

4.7.3 Negative Current Limit (Buck)

If an external source somehow drives current into V_{OUT1}, the controller attempts to regulate V_{OUT1} by reversing its inductor current to absorb the externally sourced current. If the external source is low impedance, the current may be reversed to unacceptable levels, and the controller initiates its negative current limit protection. Similar to normal overcurrent, negative current protection is enabled by monitoring the current through the lower FET. When the valley point of the inductor current reaches negative current limit, the lower FET is turned off and the upper FET is forced on until the current reaches the positive current limit or an internal clock signal is issued. At this point, the lower FET is allowed to operate. If the current is again pulled to the negative limit on the next cycle, the upper FET is again forced on, and current is forced to 1/6 of the positive current limit. At this point the controller turns off both FETs and waits for COMP1 to indicate a return to normal operation. During this time, the controller applies a 100Ω load from LX1 to PGND and attempts to discharge the output. Negative current limit is a pulse-by-pulse style operation, and its recovery is automatic.

4.7.4 Over-Temperature Protection (Buck and LDO)

Over-temperature protection limits the maximum junction temperature in the RAA212421. When the junction temperature (T_J) of the buck converter exceeds +150°C, both FETs are turned off and the controller waits for the temperature to decrease by approximately 25°C. During this time, PG1 is pulled low. When the temperature is within an acceptable range, the controller initiates a normal soft-start sequence. For continuous operation, the +125°C junction temperature rating should not be exceeded.

If the junction temperature of the LDO exceeds around +160°C, the output of the LDO shuts down until the junction temperature cools by approximately 10°C.

4.7.5 Boot Undervoltage Protection (Buck)

During PWM operation near dropout (V_{IN1} near V_{OUT1}), the regulator may hold the upper FET on for multiple clock cycles. To prevent the boot capacitor from discharging, the lower FET is forced on for approximately 200ns every 10 clock cycles.

If the boot capacitor voltage falls below 1.8V, the boot undervoltage protection circuit turns on the lower FET for 400ns to recharge the capacitor. This operation can occur during long periods of no switching, such as PFM no load situations.

4.8 Input Voltage Requirement (LDO)

The LDO of the RAA212421, a linear voltage regulator operating from 1.8V to 6V input voltage, regulates output voltage between 0.8V to 5.5V with maximum 500mA output current.

Due to the nature of an LDO, V_{IN2} must be some margin higher than V_{OUT2} plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN2} to V_{OUT2}. The generous dropout specification of the LDO allows a level of efficiency in application designs.

4.9 Enable Operation (LDO)

The ENABLE turn-on threshold is typically 800mV with 80mV of hysteresis. As a result, this pin must not be left floating and should be tied to V_{IN2} if not used. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open-drain outputs to control the EN2 pin. The EN2 pin may be connected directly to V_{IN2} for applications with outputs that are always on.

5. Application Guidelines

5.1 Simplifying the Design

Although the RAA212421 buck converter offers user programmed options for most parameters, the easiest implementation with the fewest components involves selecting internal settings for SS1, COMP1, and FS1. Table 1 on page 4 provides component value selections for a variety of output voltages and allows the designer to implement solutions with minimal effort.

5.2 Operating Frequency

The RAA212421 buck converter operates at a default switching frequency of 500kHz if the FS1 pin is tied to VCC1. Tie a resistor from the FS1 pin to GND to program the switching frequency from 300kHz to 2MHz, as shown in Equation 7.

$$R_{FS1}[k\Omega] = 108.75k\Omega*(t - 0.2\mu s)/1\mu s \quad \text{(EQ. 7)}$$

where:

t is the switching period in µs.

Figure 57 plots the desired switching frequency and its corresponding R_{FS1}.

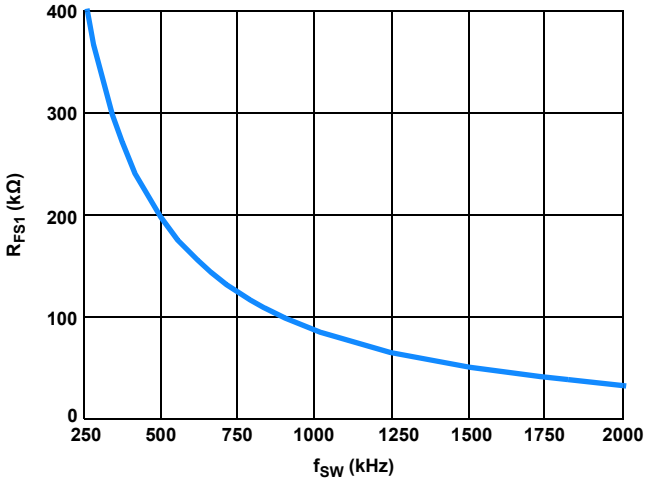


Figure 57. R_{FS1} Selection vs f_{SW}

5.3 Minimum On/Off-Time Limitation

Minimum on-time (t_{ON}) is the shortest duration of time that the HS FET can be turned on and minimum off time (t_{OFF}) is the shortest duration of time that the HS FET can be turned off. The typical t_{ON} is 90ns and the typical t_{OFF} is 150ns. For a given t_{ON} and t_{OFF}, the higher the switching frequency, the narrower the range of allowed duty cycle, which translates to a smaller allowed V_{IN} range.

For a given output voltage (V_{OUT}) and switching frequency (f_{SW}), the maximum allowed voltage is given by Equation 8:

$$V_{IN(max)} = \frac{V_{OUT}}{f_{SW} \times t_{ON}} \quad \text{(EQ. 8)}$$

The minimum allowed voltage is given by Equation 9:

$$V_{IN(min)} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF}} \quad \text{(EQ. 9)}$$

Table 2 shows the recommended switching frequencies for the various V_{OUT} to operate up to the maximum V_{IN} (40V).

Table 2. Recommended Switching Frequencies for Various V_{OUT}

$V_{IN\ (max)}$ (V)	V_{OUT} (V)	f_{SW} (kHz)
40	5	500
40	3.3	500
40	2.5	500
40	1.8	300

5.4 Synchronization Control

The frequency of operation of the buck converter can be synchronized up to 2MHz by an external signal applied to the SYNC1 pin. The rising edge on the SYNC1 triggers the rising edge of LX1. To properly synchronize, the external source must be at least 10% greater than the programmed free running IC frequency.

5.5 Output Inductor Selection

The inductor value determines the converter's ripple current. A reasonable starting point for choosing the ripple current, ΔI, is 30% of total load current. The inductor value can then be calculated using Equation 10:

$$L_1 = \frac{V_{IN1} - V_{OUT1}}{f_{SW} \times \Delta I} \times \frac{V_{OUT1}}{V_{IN1}} \quad \text{(EQ. 10)}$$

As an example, using V_{IN1} = 24V, V_{OUT1} = 5V, f_{SW} = 500kHz, I_{OUT1} = 1.1A, and $\Delta i/I_{OUT1}$ = 30%, the inductance is calculated as follows:

$$L_1 = \frac{24V - 5V}{500kHz \times 0.3 \times 1.1A} \times \frac{5V}{24V} = 24\mu H \quad \text{(EQ. 11)}$$

We can choose a standard inductance value of 22µH.

Increasing the inductance value reduces the ripple current and the ripple voltage. However, the larger inductance value may reduce the converter's response time to a load transient. The inductor current rating should not be allowed to saturate in overcurrent conditions. For typical RAA212421 applications, inductor values generally lie in the 10µH to 47µH range. Generally, higher V_{OUT1} requires higher inductance.

5.6 Output Capacitor Selection (Buck)

An output capacitor is required to filter the inductor current. The current mode control loop allows the use of low ESR ceramic capacitors enabling small solution size on the PC board. Electrolytic and polymer capacitors may also be used.

Although ceramic capacitors offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturer's datasheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published; however, an assumption of ~20% further reduction generally suffices. The result of these considerations may mean an effective capacitance 50% lower than nominal and this value should be used in all design calculations. However, ceramic capacitors are a very good choice in many applications due to their reliability and extremely low ESR.

The following equations allow calculation of the required capacitance to meet the desired ripple voltage level. Additional capacitance may be used.

(EQ. 12) $$V_{OUT1ripple} = \left(\frac{\Delta I}{8 * f_{SW} * C_{OUT1}} + \Delta I * ESR + \frac{ESL \times V_{IN1}}{L_1} \right)$$

where ΔI is the inductor's peak-to-peak ripple current, f_{SW} is the switching frequency, C_{OUT1} is the output capacitor, ESR is the equivalent series resistance of the output capacitor, ESL is the equivalent series inductance of the output capacitor, and L_1 is the output filter inductance.

5.7 Loop Compensation Design

When COMP1 is not connected to VCC1, the COMP1 pin is active for external loop compensation. The RAA212421 buck converter uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered a state variable because its peak current is constant, and the system becomes a single order system. It is much easier to design a Type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 58 on page 27 shows the small signal model of the synchronous buck regulator.

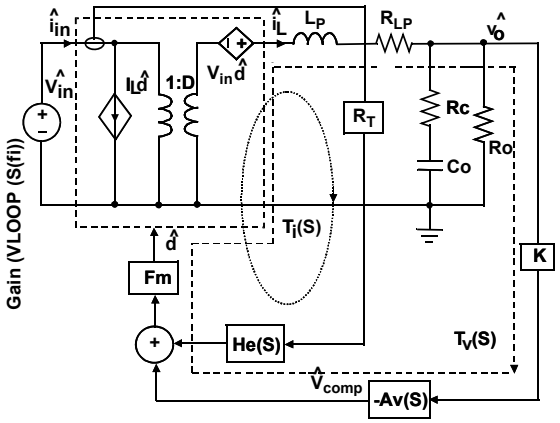


Figure 58. Small Signal Model of Synchronous Buck Regulator

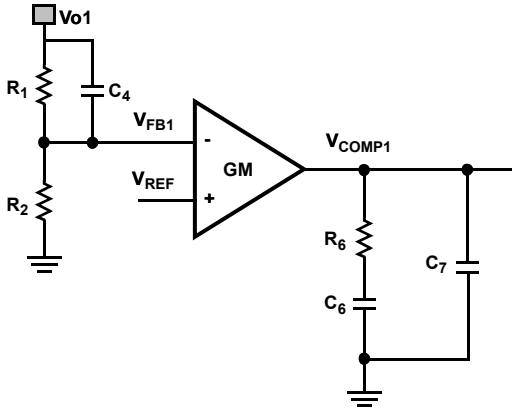


Figure 59. Type II Compensator

Figure 59 shows the type II compensator and its transfer function is expressed as shown in Equation 13:

where:

(EQ. 13) $$A_V(S)=\frac{\hat{v}_{COMP1}}{\hat{v}_{FB1}}=\frac{GM\cdot R_2}{(C_6+C_7)\cdot(R_1+R_2)}\frac{\left(1+\frac{S}{\omega_{cz1}}\right)\left(1+\frac{S}{\omega_{cz2}}\right)}{S\left(1+\frac{S}{\omega_{cp1}}\right)\left(1+\frac{S}{\omega_{cp2}}\right)}$$

$$\omega_{cz1}=\frac{1}{R_6C_6},\ \omega_{cz2}=\frac{1}{R_1C_4},\omega_{cp1}=\frac{C_6+C_7}{R_6C_6C_7},\omega_{cp2}=\frac{R_1+R_2}{C_4R_1R_2}$$

Compensator design goal:

- High DC gain
- Choose loop bandwidth f_c to be about 1/10 of f_{SW}
- Gain margin: >10dB
- Phase margin: >40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of f_c has a unity gain. Therefore, the compensator resistance R_6 is determined by Equation 14.

(EQ. 14) $$R_6=\frac{2\pi f_c V_{o1}C_{o1}R_{cs}k}{GM\cdot V_{FB1}}=16.1\times10^3\cdot f_c V_{o1}C_{o1}$$

where:

GM is the transconductance, g_m, of the voltage error amplifier in each phase.

R_{cs} is the current sense trans-resistance.

k is a constant to compensate for cross over frequency difference since the feed forward zero is placed at the vicinity of f_c.

Place the compensator zero in the vicinity of the power stage pole at full load. As an example, the compensator zero is placed at 2.2 times the frequency of the power stage pole at full load. Compensator capacitor C_6 is then given by Equation 15.

(EQ. 15) $$C_6=\frac{R_{o1}C_{o1}}{2.2R_6}=\frac{V_{o1}C_{o1}}{2.2I_{o1}R_6}$$

There is an inherent integrator pole at DC by virtue of the compensation circuit which helps to achieve high DC gain. Put another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower, in Equation 16. An optional zero can boost the phase margin. ω_{CZ2} is a zero due to R_1 and C_4.

(EQ. 16) $$C_7=\max\left(\frac{R_cC_{o1}}{R_6},\frac{1}{\pi f_{SW}R_6}\right)$$

Put feedforward zero at f_{zff} to boost the phase at cross-over. The f_{zff} can be chosen in the vicinity of f_c depending on the amount of phase boost required.

(EQ. 17) $$C_4=\frac{1}{2\pi f_{zff}R_1}$$

Example: V_{IN1} = 24V, V_{O1} = 5V, I_{O1} = 1.1A, f_{SW} = 500kHz, R_2 = 90.9kΩ, C_{o1} = 32.1µF/5mΩ, L_1 = 22µH, f_c = 50kHz, then compensator resistance R_6:

(EQ. 18) $$R_6=16.1\times10^3\cdot50kHz\cdot5V\cdot31.3\mu F=129.3k\Omega$$

Use 130kΩ as the closest standard value for R_6.

(EQ. 19) $$C_6 = \frac{5V \cdot 32.1\mu F}{1.1A \cdot 130k\Omega x 2.2} = 0.497nF$$

(EQ. 20) $$C_7 = \max\left(\frac{5m\Omega \cdot 32.1\mu F}{130k\Omega}, \frac{1}{\pi \cdot 500kHz \cdot 130k\Omega}\right) = (1.2pF, 4.9pF)$$

There is approximately 3pF parasitic capacitance from V_{COMP1} to GND; therefore, C_7 is optional. Use C_6 = 470pF and C_7 = OPEN. Choose f_{zff} to be 1.5 x f_c.

(EQ. 21) $$C_4 = \frac{1}{2\pi \cdot 50kHz \cdot 1.5 \cdot 90.9k\Omega} = 23.3pF$$

Use C_4 = 22pF. Figure 60 on page 29 shows the simulated voltage loop gain, which has a 44kHz loop bandwidth with an 84° phase margin and 21dB gain margin. In the above example, 22µF+47µF 1206 case size ceramic capacitors are used. The effective output capacitance after voltage derating is 32.1µF. In practice, ceramic capacitors have significant derating on voltage and temperature depending on the type. See the ceramic capacitor datasheet for more details.

The previous description is one of the methodologies to design the compensation network and can be used as a general guideline. However, it is not the only way to choose compensation components. The optimal compensation components may vary depending on the user's requirements.

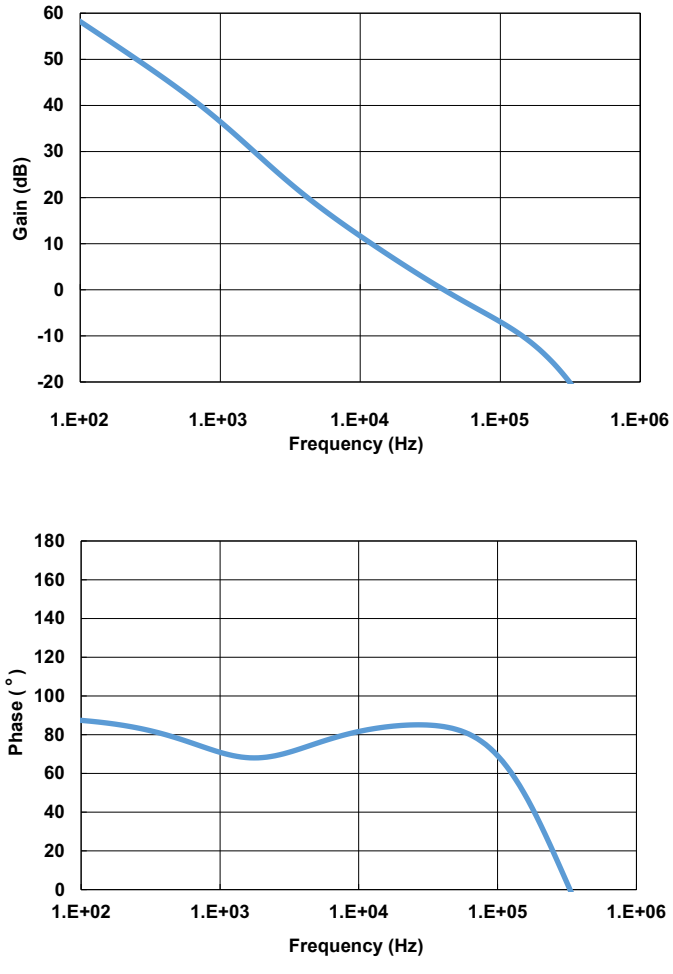


Figure 60. Simulated Loop Gain

5.8 External Capacitor Requirements (LDO)

For the most recent package outline drawing, see L22.3x6.

External capacitors are required for proper operation. Pay careful attention to the layout guidelines and selection of capacitor type and value to ensure optimal performance.

5.8.1 Output Capacitor

The RAA212421 LDO applies state-of-the-art internal compensation to keep the selection of the output capacitor simple for the customer. Stable operation over full temperature, V_{IN2} range, V_{OUT2} range, and load extremes are ensured for all capacitor types and values assuming a minimum of 4.7µF X5R/X7R is used for local bypass on V_{OUT2}. This output capacitor must be connected to the V_{OUT2} and GND pins of the LDO with PCB traces no longer than 0.5cm.

There is a growing trend to use very low ESR Multilayer Ceramic Capacitors (MLCC) because they can support fast load transients and bypass very high frequency noise from other sources. However, the effective capacitance of MLCCs drops with applied voltage, age, and temperature.

Additional capacitors of any value in ceramic, POSCAP, or alum/tantalum electrolytic types may be placed in parallel to improve PSRR at higher frequencies and/or load transient AC output voltage tolerances.

5.8.2 Input Capacitor

For proper operation, a minimum capacitance of 4.7µF X5R/X7R is required at the LDO input. This ceramic input capacitor must be connected to the V_{IN2} and GND pins of the LDO with PCB traces no longer than 0.5cm.

5.8.3 Phase Boost Capacitor

A small phase boost capacitor, C_{PB}, can be placed across the top resistor, R_3, in the feedback resistor divider network to improve the AC performances of the LDO for the applications in which the output capacitor is 10µF or larger. For 10µF output capacitor, the recommended C_{PB} value can be calculated by using Equation 22.

(EQ. 22) $$C_{PB} = \frac{1}{2\pi x 27000 x R_1}$$

This zero increases the LDO crossover frequency and provides additional phase resulting in faster load transient response.

5.9 Power Dissipation and Thermals

The junction temperature must not exceed the range specified in the "Recommended Operating Conditions" on page 7. The power dissipation can be calculated by using Equation 23:

(EQ. 23) $$P_D = (V_{IN2} - V_{OUT2}) \times I_{OUT2} + V_{IN2} \times I_{GND}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$, determine the maximum allowable power dissipation, as shown in Equation 24:

(EQ. 24) $$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

θ_{JA} is the junction-to-ambient thermal resistance.

For safe operation, ensure that the power dissipation P_D, calculated from Equation 23, is less than the maximum allowable power dissipation $P_{D(MAX)}$.

6. Layout Considerations

Proper layout of the power converter minimizes EMI and noise, and ensure first pass success of the design. PCB layouts are provided in multiple formats on the Renesas web site. In addition, Figure 61 illustrates the important points in PCB layout. In reality, PCB layout of the RAA212421 is quite simple.

- A multilayer PCB with GND plane is recommended. Figure 61 shows the placement of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent multiple physical capacitors. The most critical connections are to tie the GND1 and GND2 pins to the package GND pad and then use vias to directly connect the GND pad to the system GND plane. This connection of the GND pad to system plane ensures a low impedance path for all return current, as well as an excellent thermal path to dissipate heat. With this connection made, place the high frequency MLCC input capacitor near the V_{IN1} pin and use vias directly at the capacitor pad to tie the capacitor to the system GND plane.
- Place a 1µF MLCC near the VCC1 pin and directly connect its return with a via to the system GND plane.
- Place the feedback divider close to the FB1 pin and do not route any feedback components near LX1 or BOOT1. If external components are used for SS1, COMP1, or FS1, the same advice applies.

The performance of the LDO depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum performance:

- A minimum capacitance of 4.7µF X5R/X7R ceramic input capacitor must be placed to the VIN2 and GND pins of the LDO with PCB traces no longer than 0.5cm
- A minimum capacitance of 4.7µF X5R/X7R ceramic output capacitor must be placed to the VOUT2 and GND pins of the LDO with PCB traces no longer than 0.5cm
- Connect the EPAD to the ground plane with low-thermal resistance vias

An example component placement is shown in Figure 61.

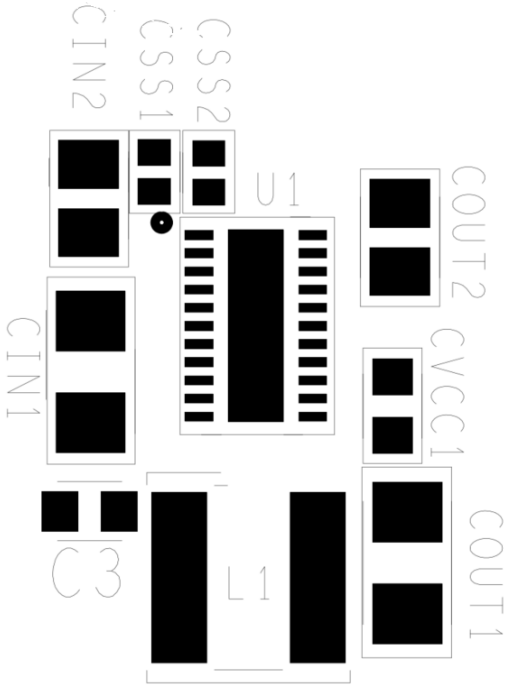


Figure 61. Printed Circuit Board Example Component Placement

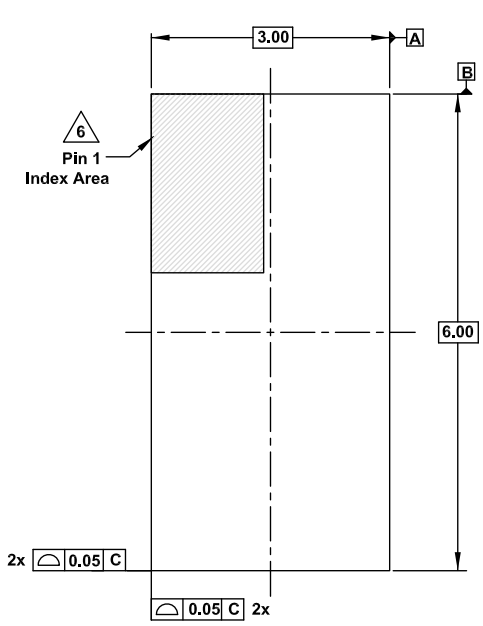
7. Revision History

Rev.	Date	Description
3.00	Jul 8, 2019	Updated page 1 description. Updated Features section. Updated Figures 2,3, 4, and 5. Updated SYNC1 pin description. Added PFM Peak Current Limit spec on page 9. Updated “Typical Performance Curves”. Added “Light Load Operation” on page 21. Updated Boot Undervoltage Protection (Buck) section. Added Minimum On/Off-Time Limitation section.
2.00	Dec 13, 2018	Updated ordering information table. Updated Layout Considerations section. Updated disclaimer.
1.00	Sep 24, 2018	Updated the output current from 1.2 to 1.1 through out the document. Updated Figures 2, 6, 7, 8, 9 and 19 (label only for this one). Added text and Equation 8 in Section 5.4. Updated Equations 12 and 15.
0.00	Sep 7, 2018	Initial release.

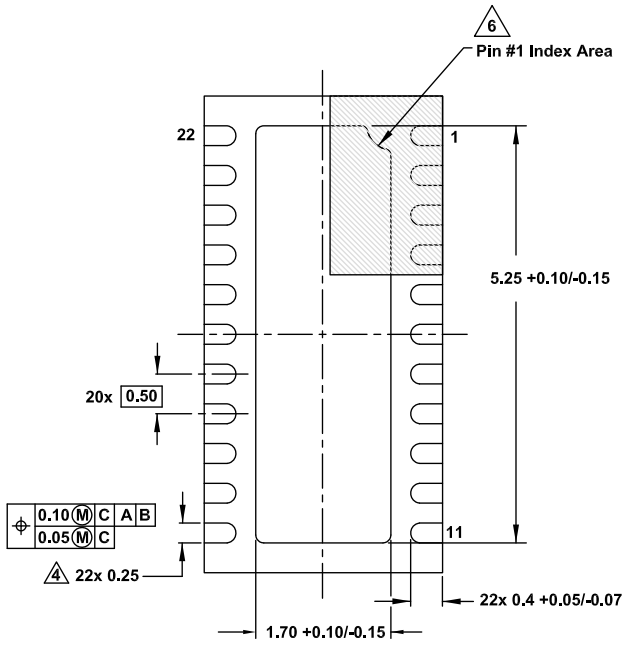
8. Package Outline Drawing

For the most recent package outline drawing, see L22.3x6.

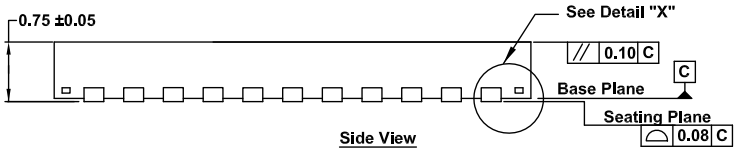
L22.3x6
22 Lead Thin Dual Flat No-Lead Plastic Package (TDFN)
Rev 0, 3/18



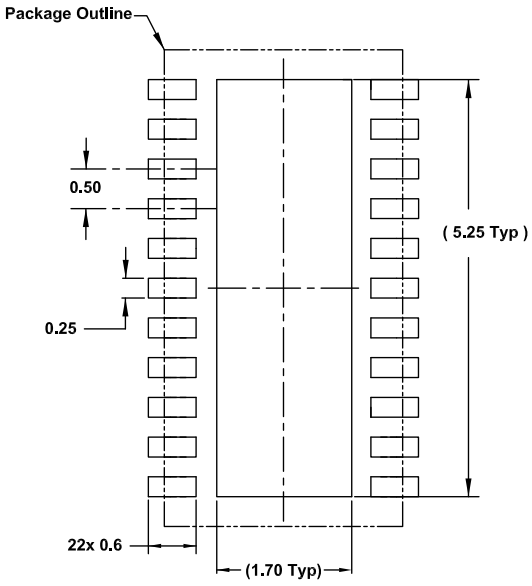
Top View



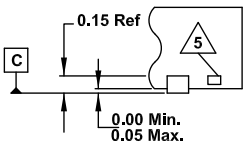
Bottom View



Side View



Typical Recommended Land Pattern



Detail "X"

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.20mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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