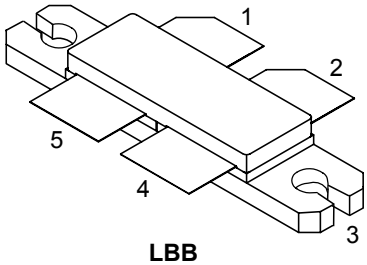
RF5L15120CB4

Datasheet

120 W 50 V RF power LDMOS transistor from HF to 1.5 GHz



LBB

Pin connection	
Pin	**Connection**
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

STPOWER

Product status link
RF5L15120CB4

Product summary	
Order code	RF5L15120CB4
Marking	RF5L15120CB4
Package	LBB
Packing	Tape and reel 13"
Base/bulk quantity	100/100

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF5L15120CB4	1000 MHz	50 V	120 W	20 dB	60%

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate/source voltage range
- Excellent thermal stability, low HCI drift
- In compliance with the european directive 2002/95/EC

Applications

- Broadband commercial communications
- TV broadcast
- Avioncs
- Industrial

Description

The RF5L15120CB4 is a 120 W LDMOS FET, designed for broadband commercial communications, TV Broadcast, Avionics and industrial applications with frequencies from HF to 1.5 GHz. It can be used in class AB/B and class C for all typical modulation formats.

1 Electrical data

1.1 Absolute ratings

Table 1. Absolute maximum ratings (T_{CASE}= 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	95	V
V_{GS}	Gate-source voltage	-8/+10	V
V_{DD}	Maximum operating voltage	55	V
T_J	Maximum junction temperature	+200	°C
T_{STG}	Storage temperature range	-65 to +150	°C

1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Junction-case thermal resistance	0.7	°C/W

Note: *T_{CASE} = +85 °C , T_J = +200 °C, DC test.*

1.3 ESD protection characteristics

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (per JESD22-A114)	2

2 Electrical characteristics

2.1 Static

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_{DS} = 0.5 mA	95			V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 90 V			1	µA
		V_{GS} = 0 V, V_{DS} = 50 V				
I_{GSS}	Gate-source leakage current	V_{GS} = 10 V, V_{DS} = 0 V			100	nA
		V_{GS} = -8 V, V_{DS} = 0 V				
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 50 V, I_{DS} = 600 µA	2		2.8	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 50 V, I_{DS} = 400 mA	2		6	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_{DS} = 2 A			1.2	V
$I_{DS(on)}$	Static drain-source on-current	V_{GS} = 10 V, V_{DS} = 100 mV			2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, V_{DS} = 100 mV			1	Ω
C_{ISS}	Common source input capacitance	V_{GS} = 0 V, V_{DD} = 50 V, f = 1 MHz		56		pF
C_{RSS}	Common source feedback capacitance			0.6		pF
C_{OSS}	Common source output capacitance			23		pF

2.2 Dynamic

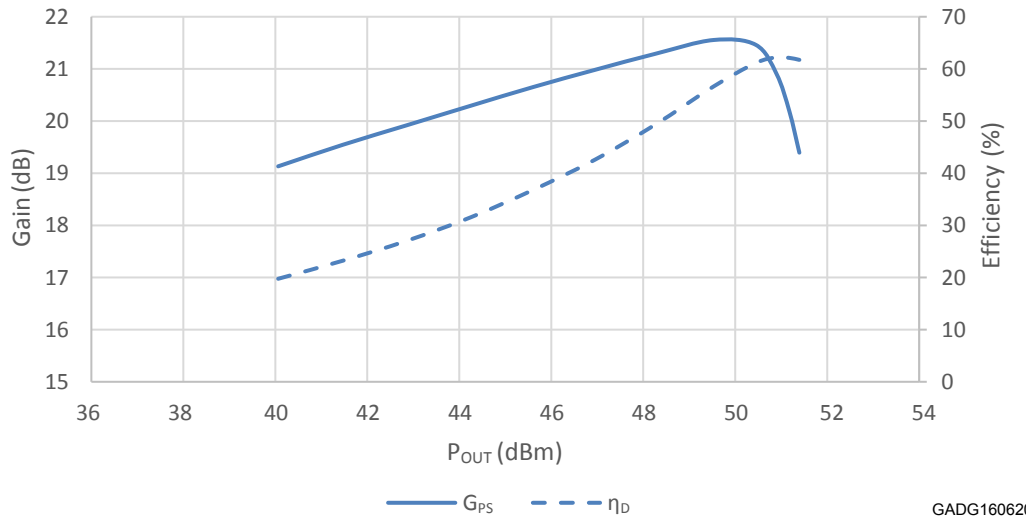
Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency				1500	MHz
P_{OUT}	Output power	f = 1000 MHz, at 1dB compression point, pulsed CW		120		W
G_{PS}	Power gain			20		dB
η_D	Drain efficiency			60		%
VSWR	Load mismatch	At 120 W pulsed CW output power, all phase angles			10:1	

Note: V_{DD} = 50 V, I_{DQ} = 100 mA, pulse width = 100 µs, duty cycle = 10%.

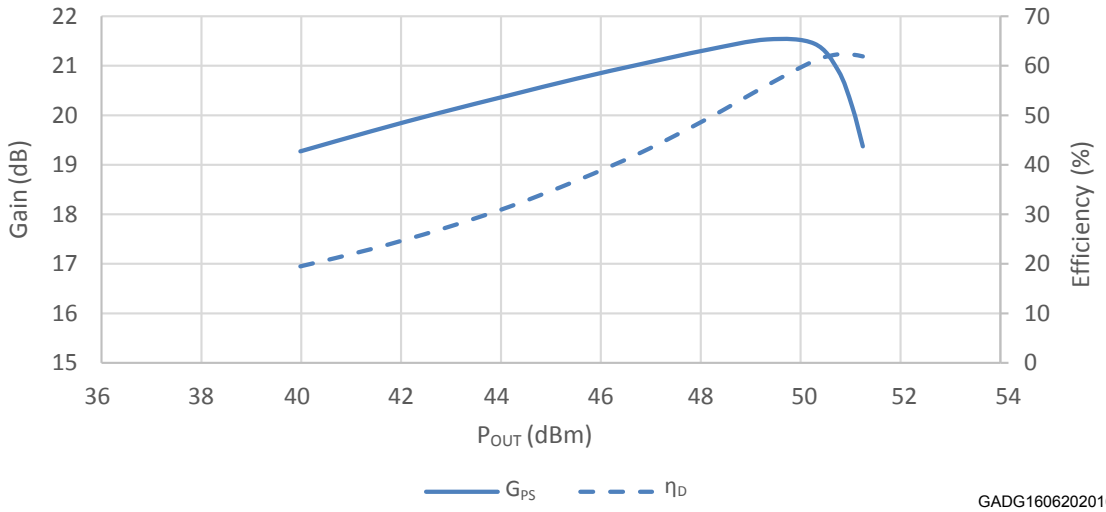
3 Typical performances

Figure 1. Power gain and drain efficiency versus output power (f = 1000 MHz, pulsed CW)



Note: V_{DD} = 50 V, I_{DQ} =100 mA, pulsed CW; pulse width = 100 µs, duty cycle = 10%.

Figure 2. Power gain and drain efficiency versus output power (f = 1000 MHz, CW)



Note: V_{DD}= 50 V, I_{DQ}= 100 mA.

4 Test circuit

4.1 Test circuit layout

Figure 3. **Test circuit layout (f = 1000 MHz)**

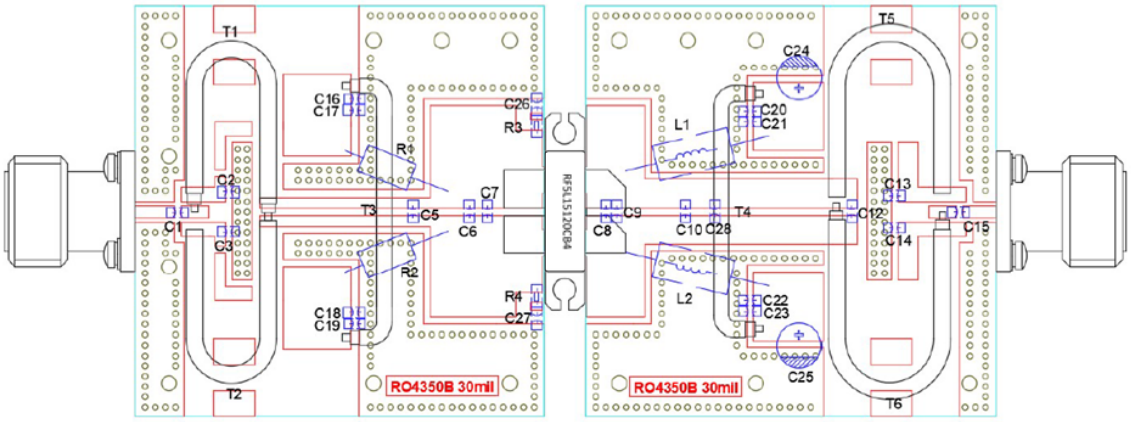


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Figure 4. **Test circuit photo (f = 1000 MHz)**

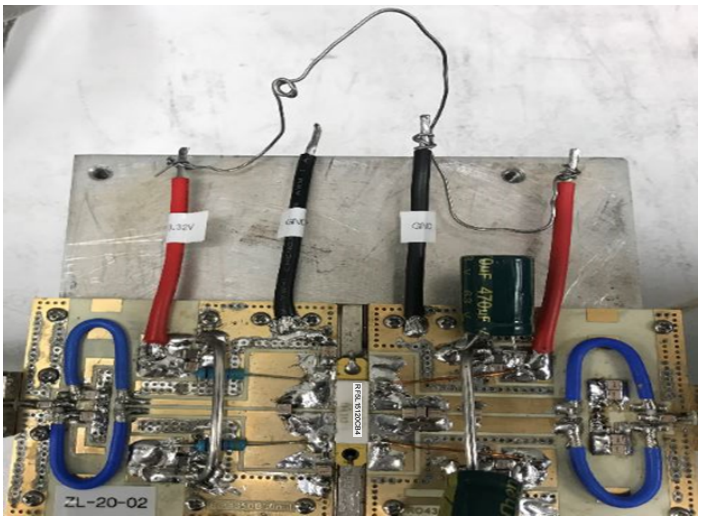

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Table 6. Components list

Component	Description	Suggested manufacturer
C1, C2, C3, C13, C14, C15, C17, C18, C21, C22, C26, C27	120 pF	ATC800B
C5	6.8 pF	ATC800B
C6	5.6 pF	ATC800B
C7	10 pF	ATC800B
C12	3.3 pF	ATC800B
C8, C9, C10, C28	8.2 pF	ATC800B
C16, C19, C20, C23	Ceramic multilayer capacitor, 10 µF, 100 V	10 µF/100 V
R1, R2	Metal film resistor, 200 Ω	
R4, R5	Chip resistor, 13 Ω, 1206	
L1, L2	Copper wire, cross section diameter 0.8 mm	
C24, C25	Electrolytic capacitor, 470 µF, 63 V	
PCB	0.762 mm [0.030"] thick, Ɛr= 3.48, Rogers RO4350B, 1 oz. copper	

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 LBB package information

Figure 5. LBB package outline

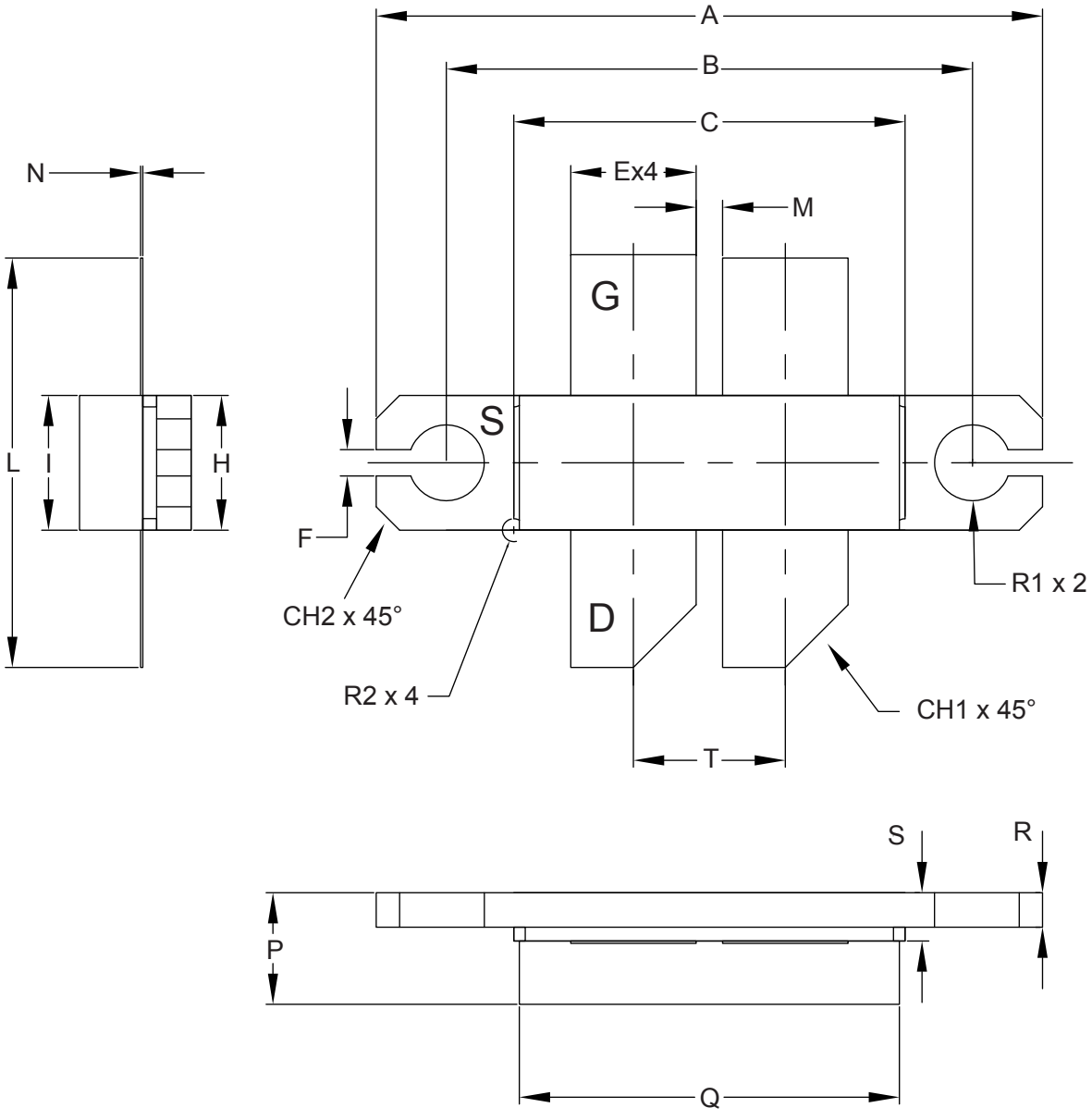

Table 7. **LBB mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
A	28.82	28.95	29.08
B	22.73	22.86	22.99
C	16.87	17.00	17.13
E	5.32	5.45	5.58
F	1.01	1.14	1.27
H	5.72	5.85	5.98
I	5.72	5.85	5.98
L	17.65	17.78	17.91
M	1.02	1.15	1.28
N		0.10	
P	4.72	4.85	4.98
Q	16.38	16.51	16.64
R	1.37	1.50	1.63
S	1.97	2.10	2.23
T		6.60	
CH1		2.72	
CH2		1.02	
R1		1.65	
R2		0.50	

Revision history

Table 8. **Document revision history**

Date	Version	Changes
16-Jun-2020	1	First release

Contents

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