S1D13719 Mobile Graphics Engine

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The S1D13719 is a Mobile Graphics Engine solution designed with support for the digital video revolution in mobile products. The S1D13719 contains an integrated dual port camera interface, hardware JPEG encoder/decoder and can be interfaced to an external MPEG codec. Seamlessly connecting to both direct and indirect CPU interfaces, it provides support for up to two LCD panels. The Mobile Graphics Engine supports all standard TFT panel types and many extended TFT types, eliminating the need for an external timing control IC. The S1D13719, with it's 512K bytes of embedded SRAM and rich feature set, provides a low cost, low power, single chip solution to meet the demands of embedded markets requiring Digital Video, such as Mobile Communications devices and Palm-size PDAs.

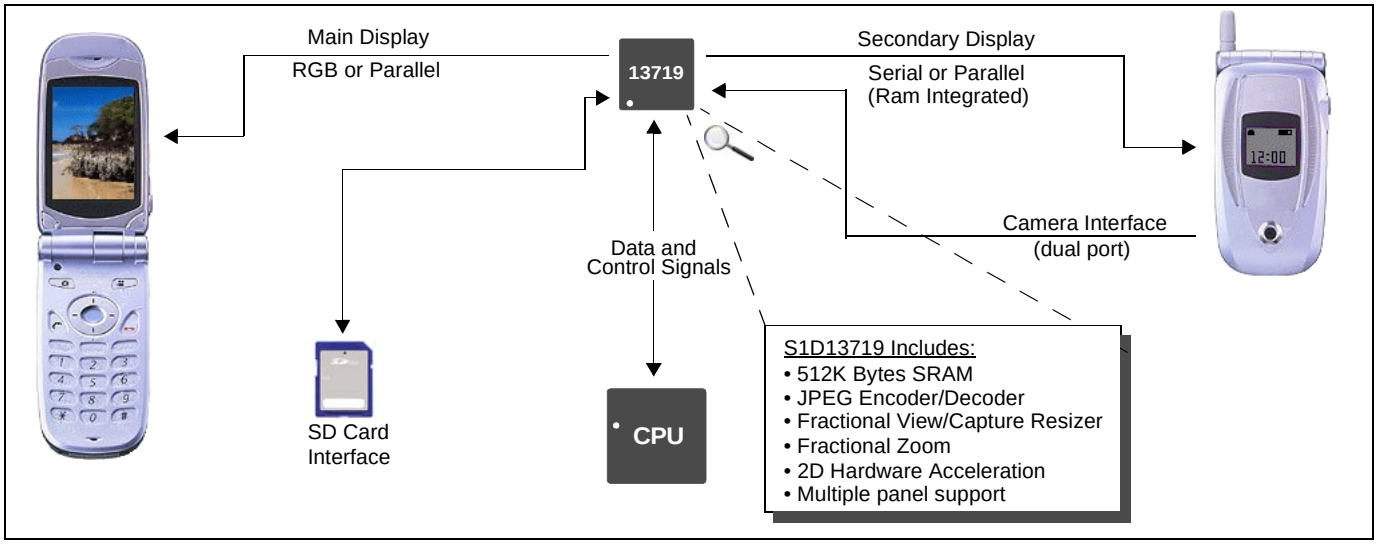
Additionally, products requiring a rotated display can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. The S1D13719 also provides support for "Picture-in-Picture Plus" (a variable size window with overlay functions). Higher performance is provided by the Hardware Acceleration Engine which provides 2D BitBLT functions.

The S1D13719 provides impressive support for cellular and other mobile solutions requiring Digital Video support. However, its impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

FEATURES

- Embedded 512K byte SRAM Display Buffer
- Low Operating Voltage
- Direct and Indirect CPU interfaces
- Programmable resolutions and color depths
- Support for 2 panels (LCD2 must be RAM integrated)
- Support for RGB, Serial and Parallel I/F Panels
- Extended TFT interfaces including HR-TFT
- Internal PLL or digital clock input
- SD Memory Card interface
- Dual port Camera interface
- Fractional View and Capture hardware resizer, reduction from 1x to ½x size in 128 steps
- Fractional Zoom for YUV 4:2:2, expand from 1x to 2x size in 128 steps
- Hardware JPEG encoder/decoder
- YUV to RGB converter
- SwivelView™ (90°, 180°, 270° hardware rotation of displayed image)
  - (Patent # 5,734,875 - Patent # 5,956,049 - Patent #6,262,751)
- "Picture-in-Picture Plus"
- 2D Hardware Acceleration Engine
- Software Initiated Power Save Mode

SYSTEM BLOCK DIAGRAM



■ DESCRIPTION

Integrated Display Buffer

- 512K bytes of embedded SRAM
- Addressable as a single linear address space

CPU Interface

- 16-bit Generic Asynchronous CPU interface
- Direct and Indirect addressing

Panel Support

- Supports up to 2 LCD panels
- LCD1: 9/12/18/24-bit RGB panel
  LCD2: 8/9-bit Serial Ram Integrated panel
- LCD1: 8/16/18/24-bit Parallel Ram Integrated panel
  LCD2: 8/9-bit Serial Ram Integrated panel
- LCD1: 8/16/18/24-bit Parallel Ram Integrated panel
  LCD2: 8/16/18/24-bit Parallel Ram Integrated panel
- LCD1: 9/12/18/24-bit RGB panel
  LCD2: 8-bit Parallel Ram Integrated panel
- TFT, HR-TFT, Casio TFT, α-TFT, ND-TFD, and Extended TFT
- Typical resolution of:
  up to 320x480 at 16 bpp
  up to 320x240 at 32 bpp

Acceleration

- 2D BitBLT Engine
- SwivelView: 90°, 180°, 270° hardware rotation of displayed image
- Mirror Display: hardware “mirror” image of display

Display Features

- 8/16/32 bit-per-pixel (bpp) support
- Picture-in-Picture Plus: displays a variable size window overlaid over the background image
- Overlay Functions
- Pixel Doubling: doubles the effective resolution
- Video Invert: inverts display data

Digital Video

- Dual port Camera Interface (YUV 4:2:2)
- Hardware JPEG Encoder (YUV 4:2:2, 4:1:1, 4:2:0)
- Hardware JPEG Decoder (YUV 4:4:4, 4:2:2, 4:1:1, 4:2:0)
- YUV Display/Capture (YUV 4:2:2, 4:2:0)
- Memory Image JPEG Encode (YUV 4:2:2, 4:1:1, 4:2:0)
- View and Capture hardware resizer, reduction from 1x to ½x size in 128 steps with trimming functions
- Fractional Zoom for YUV 4:2:2, expand from 1x to 2x size in 128 steps
- YUV to RGB and RGB to YUV converters
- Support for external MPEG codec interface

Miscellaneous

- Internal PLL or digital clock input
- Software initiated power save mode
- $CORE_{VDD}$ 1.8 volts and IO_{VDD} 3.0 volts
- PFBGA 180-pin package
- FCBGA 240-pin Package

CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- S1D13719 Technical Documentation
- S1D13719 Evaluation Boards
- CPU Independent Software Utilities
- Royalty Free source level driver code

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